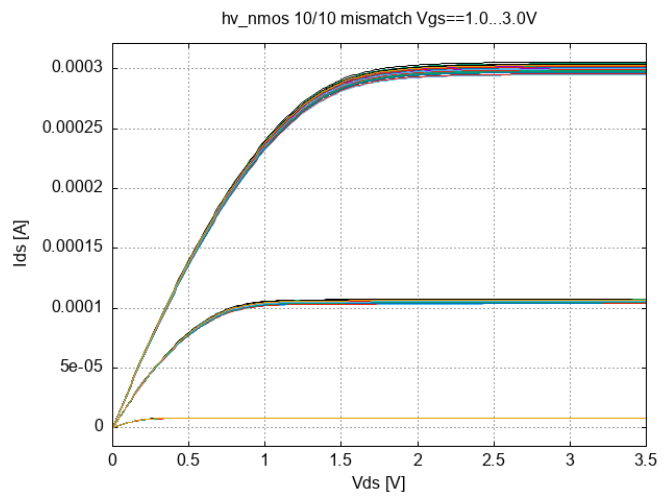
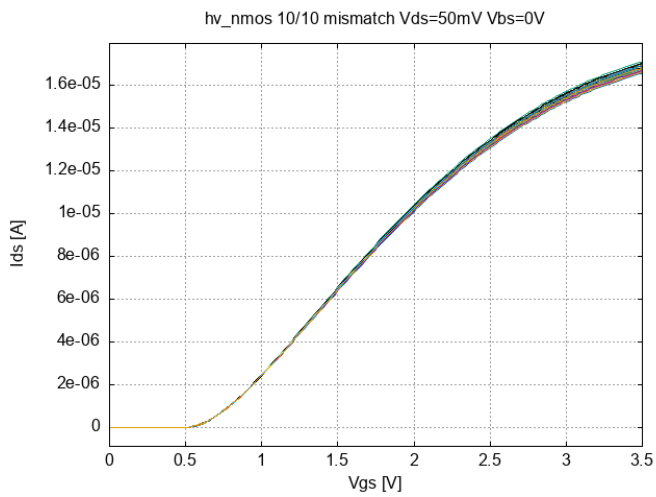
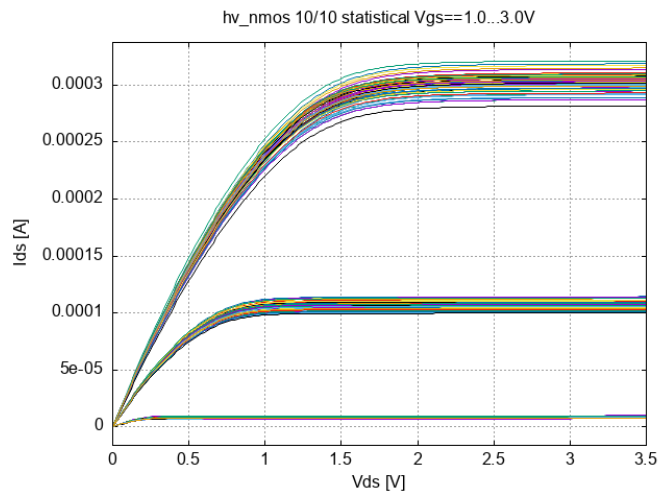
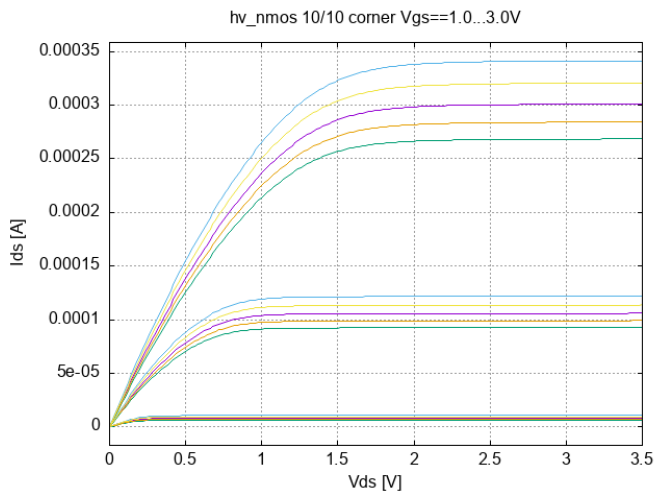
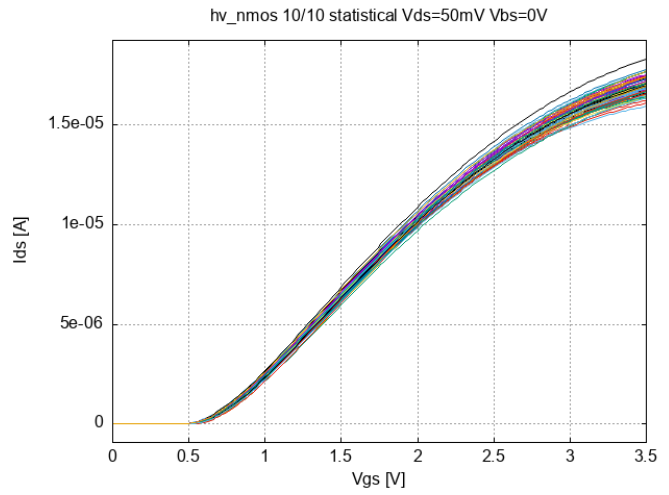
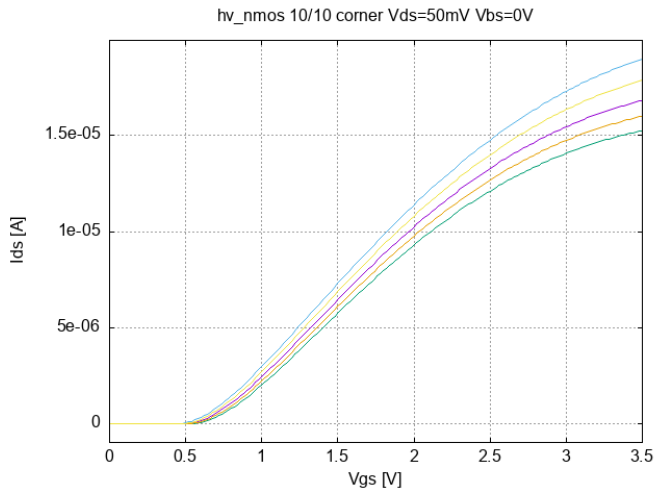
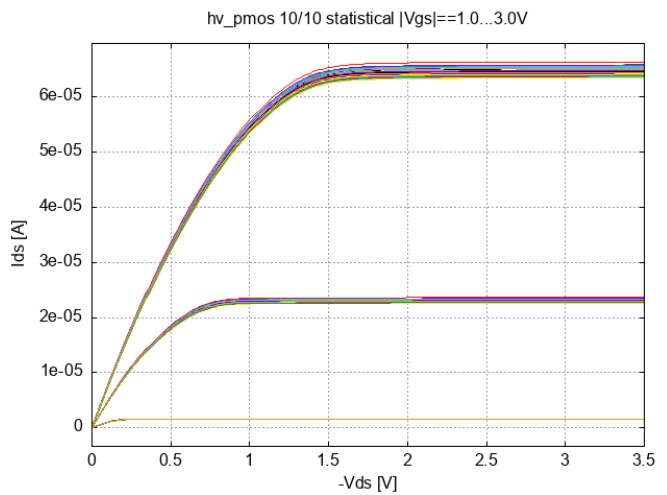
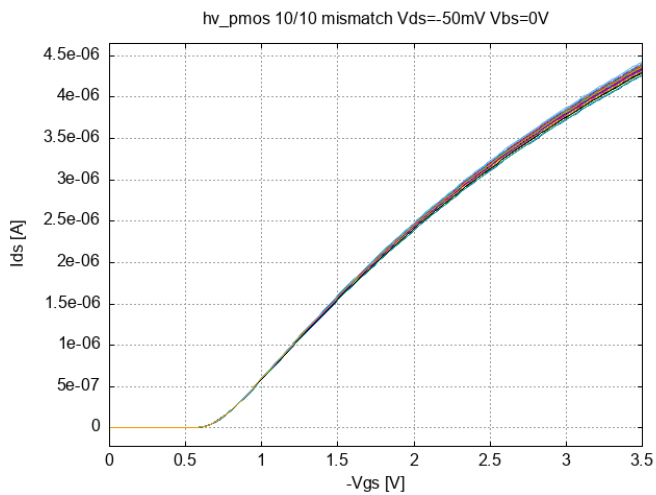
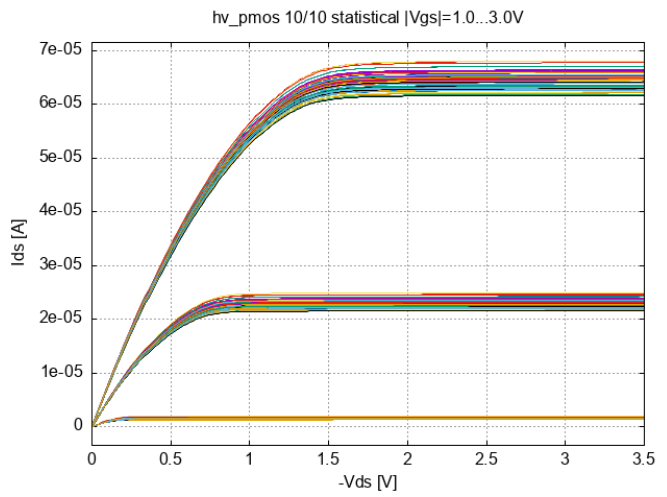
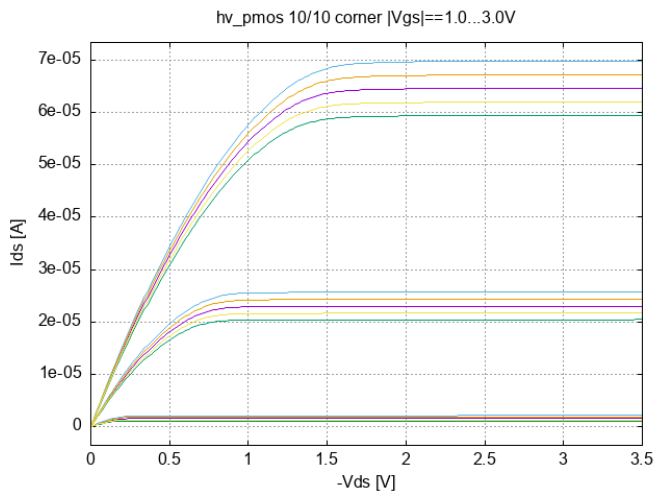
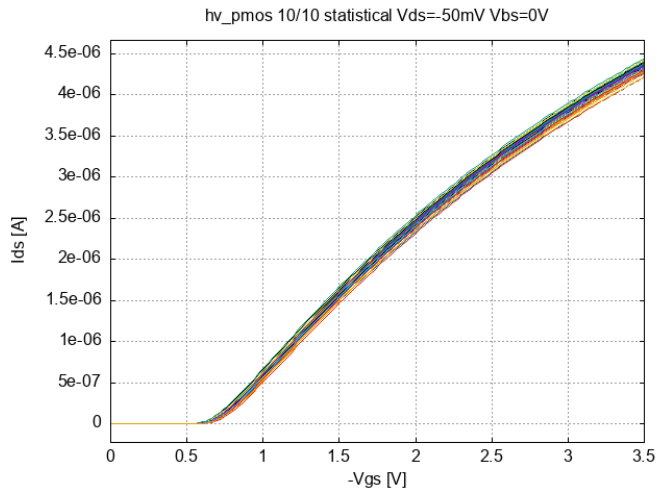
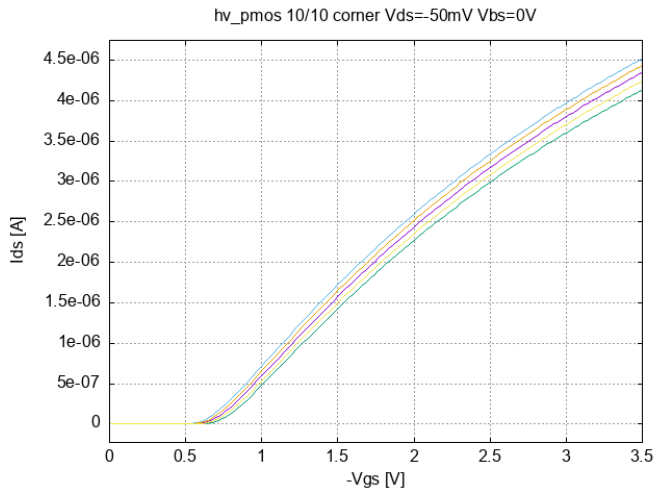


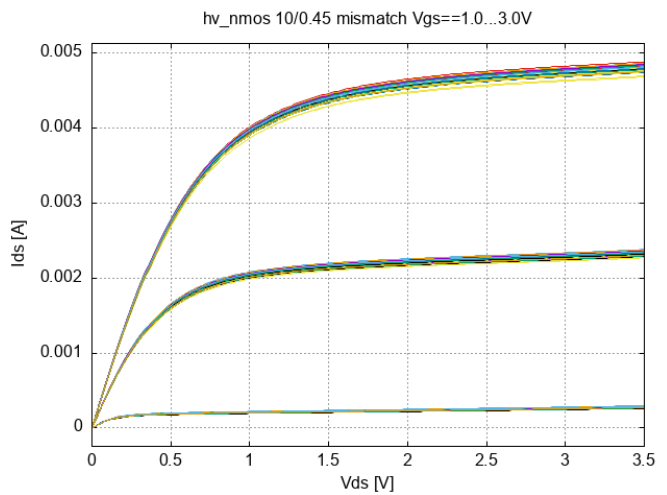
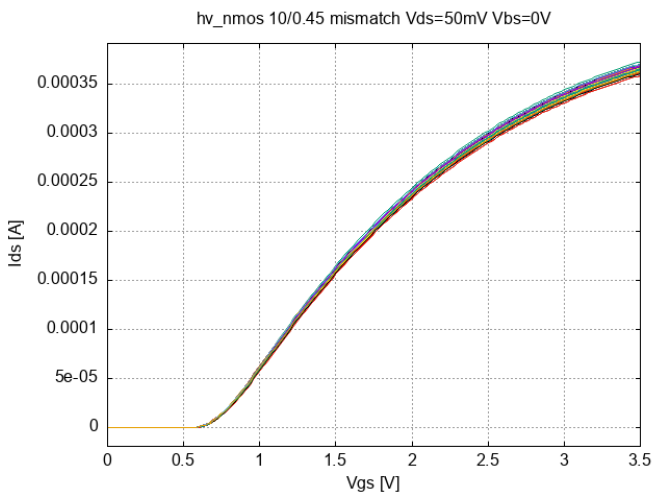
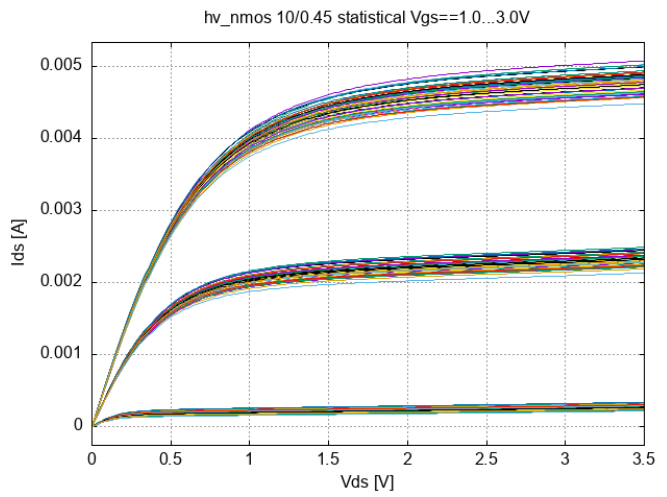
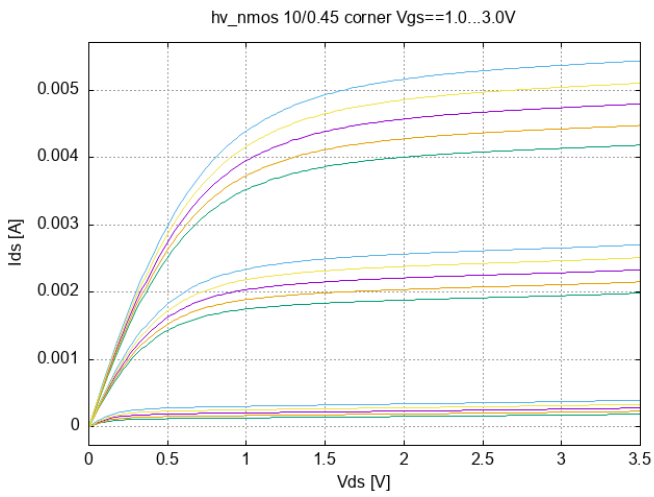
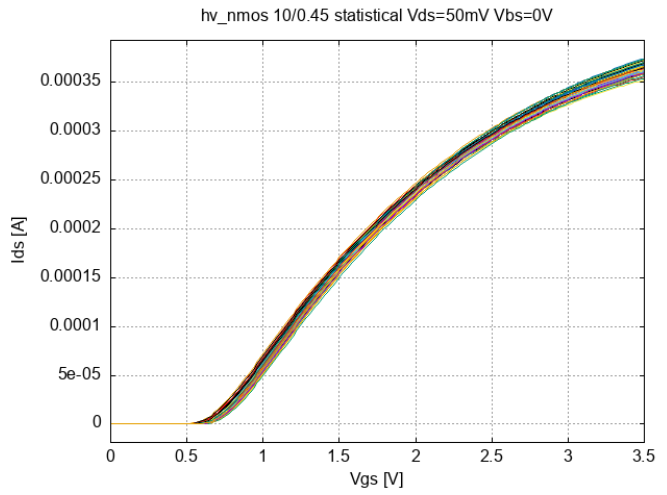
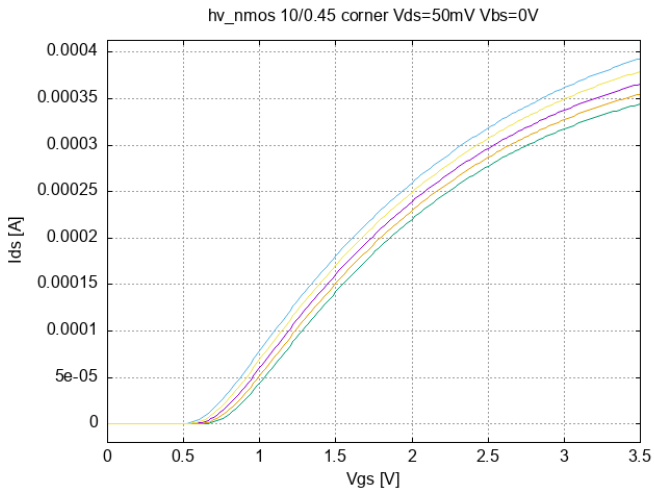
hv_nmos 10u/10u



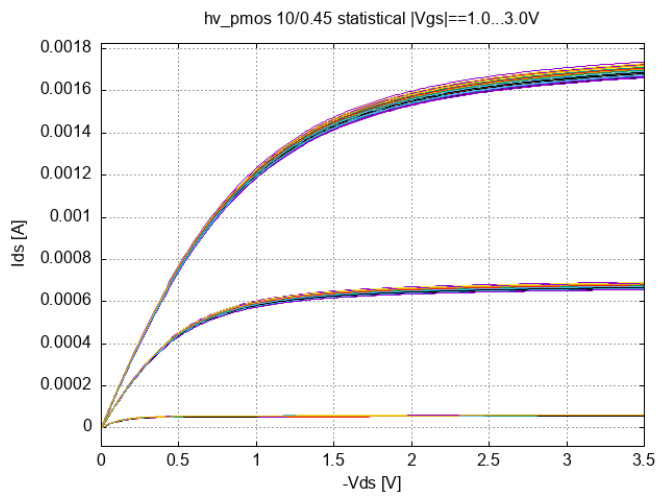
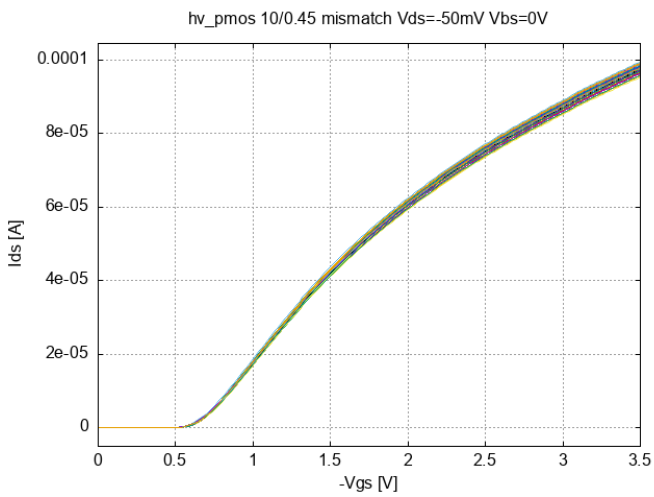
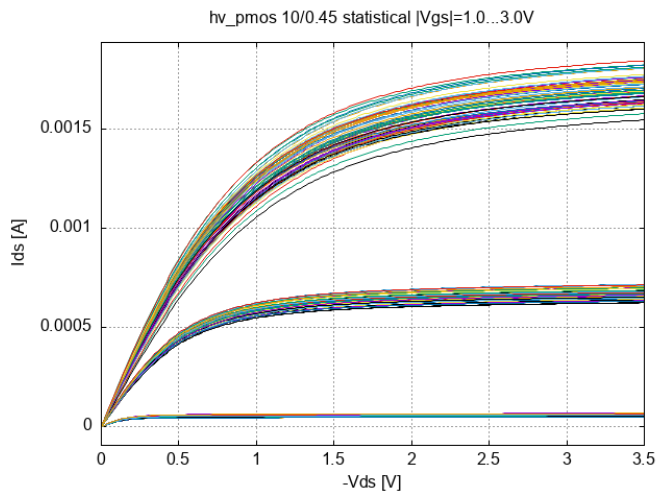
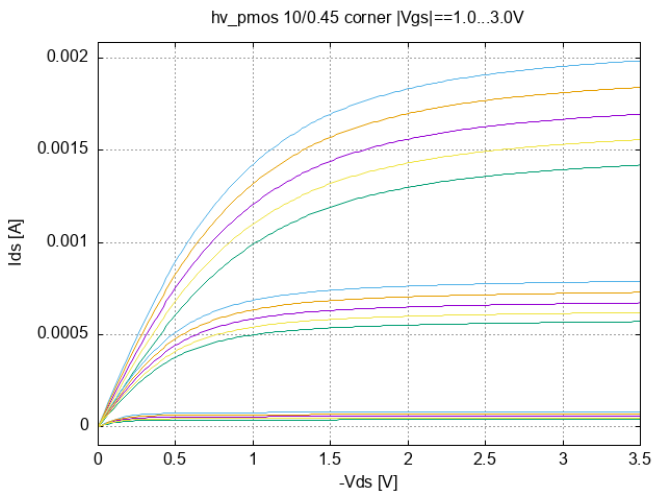
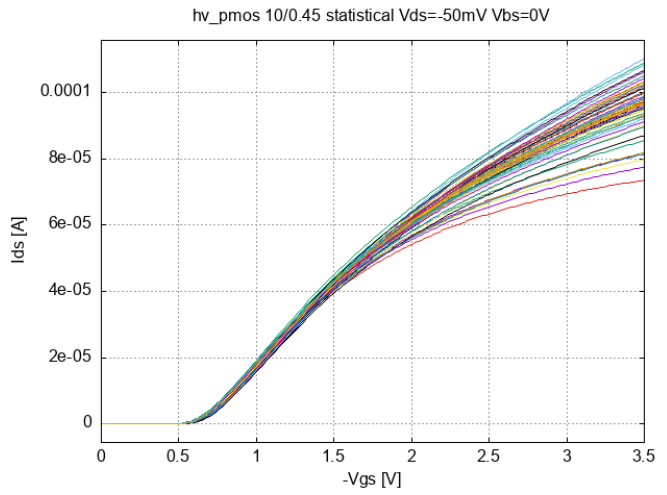
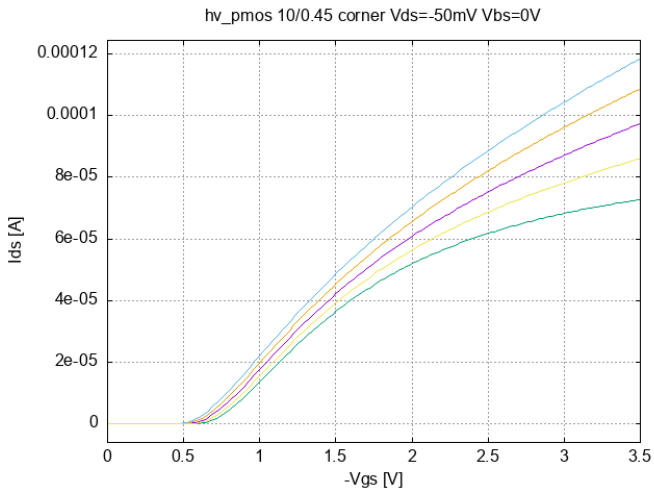
hv_pmos 10u/10u



hv_nmos 10u/0.45u

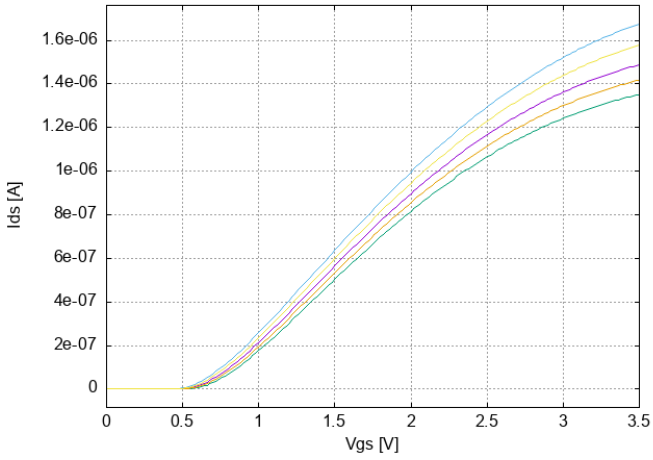


hv_pmos 10u/0.45u

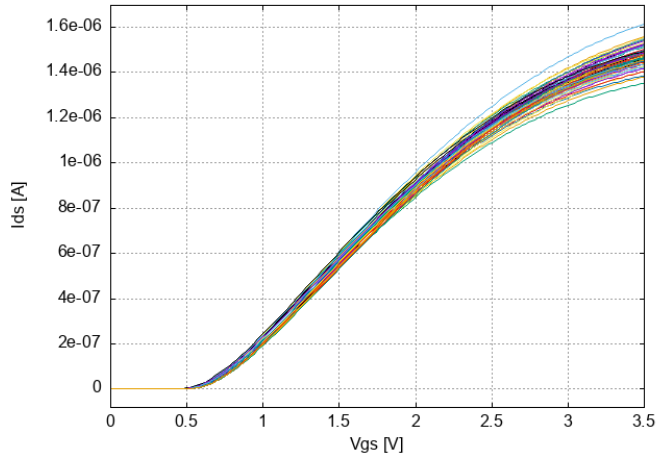


hv_nmos 1u/10u

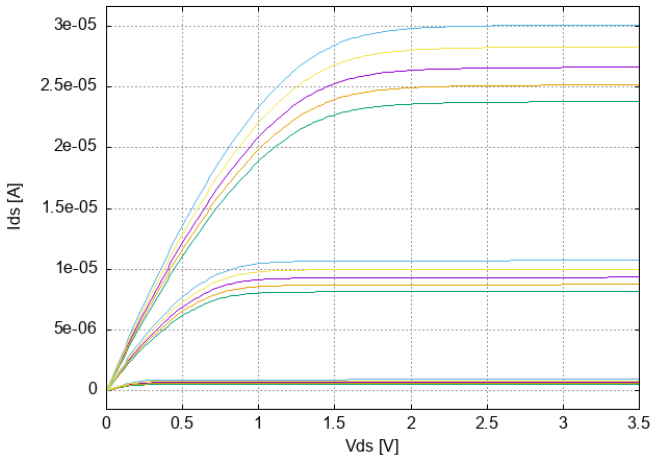
hv_nmos 1/10 corner Vds=50mV Vbs=0V



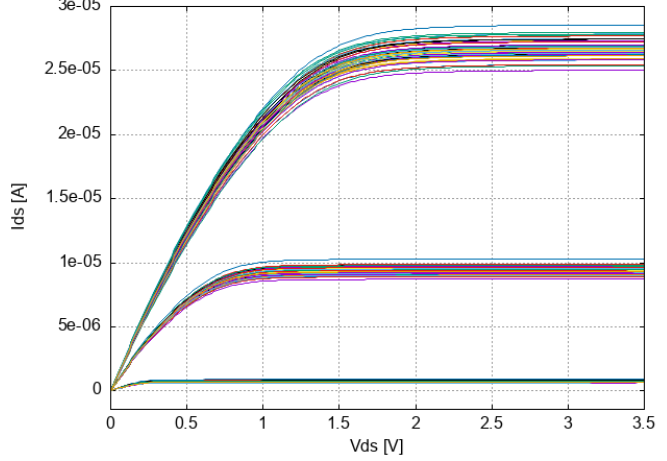
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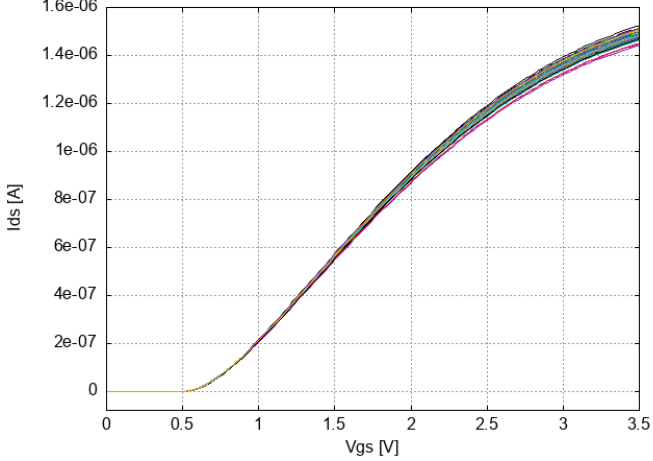
hv_nmos 1/10 corner Vgs==1.0...3.0V



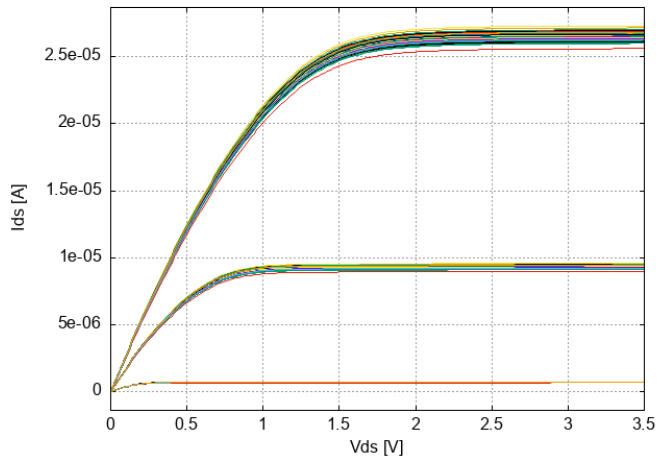
hv_nmos 1/10 statistical Vgs==1.0...3.0V



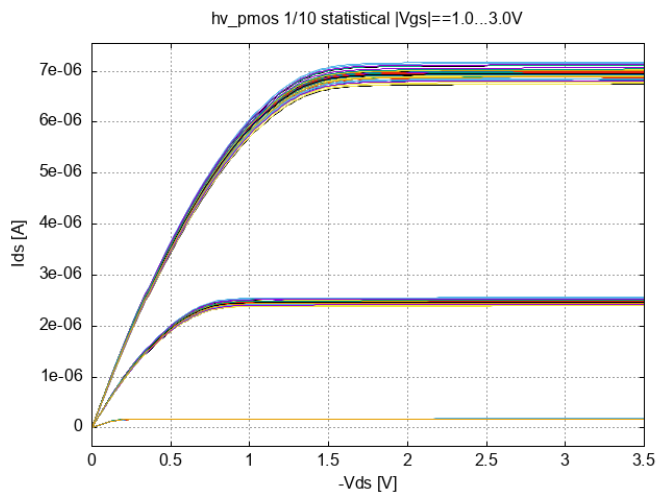
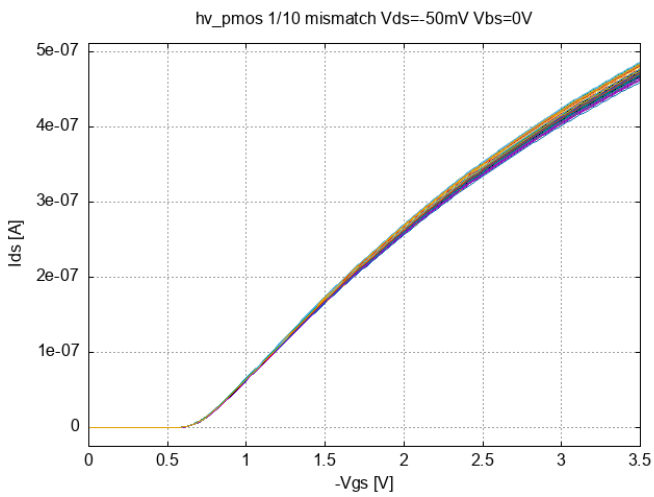
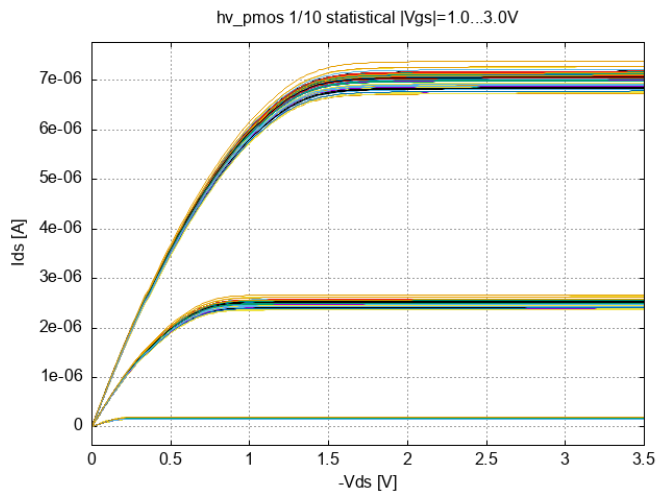
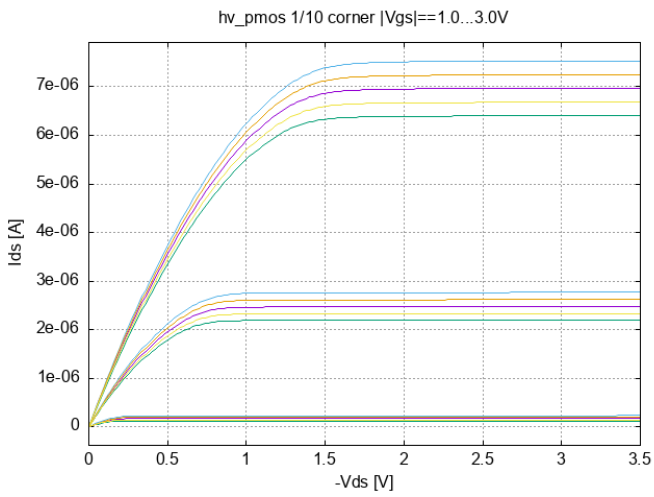
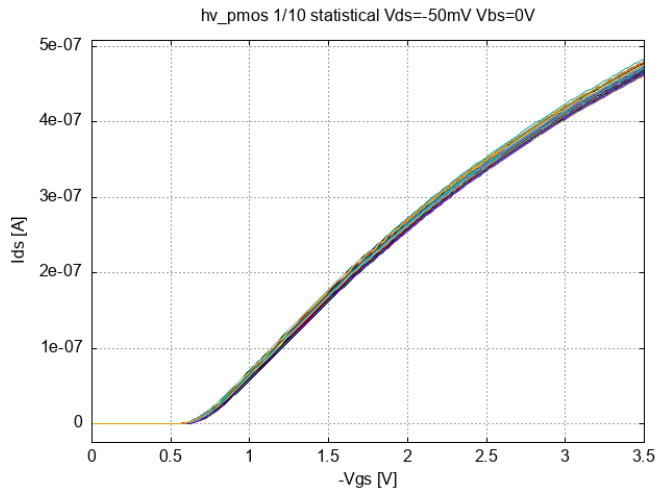
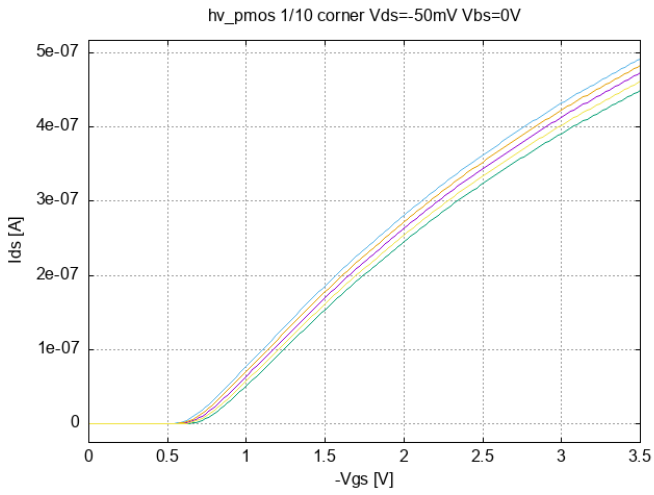
hv_nmos 1/10 mismatch Vds=50mV Vbs=0V



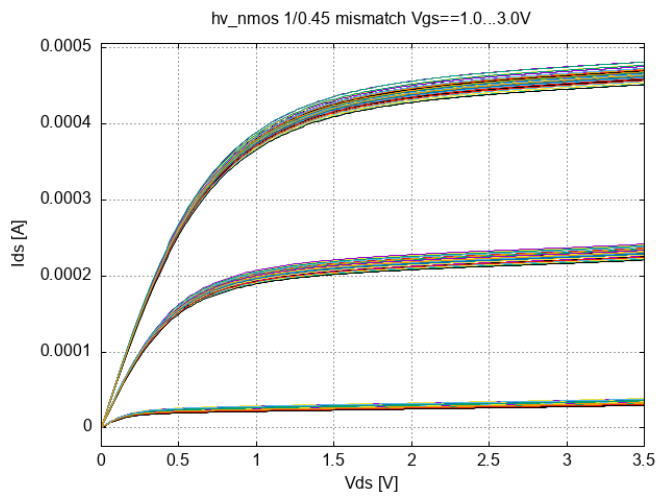
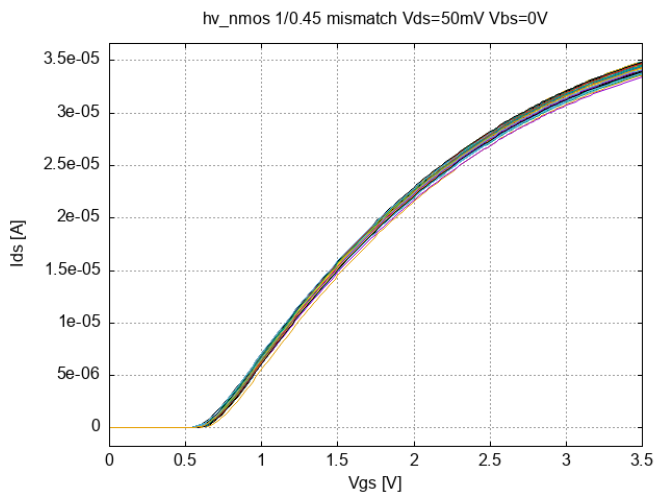
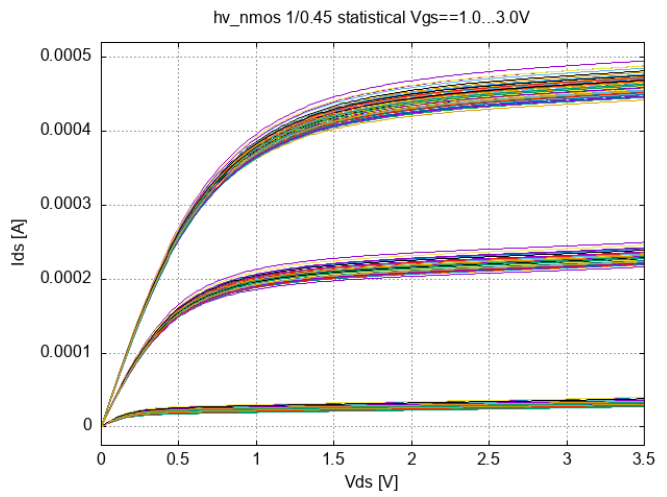
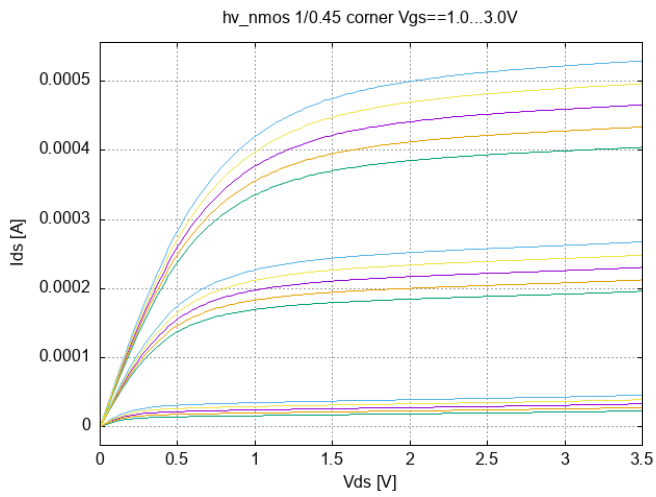
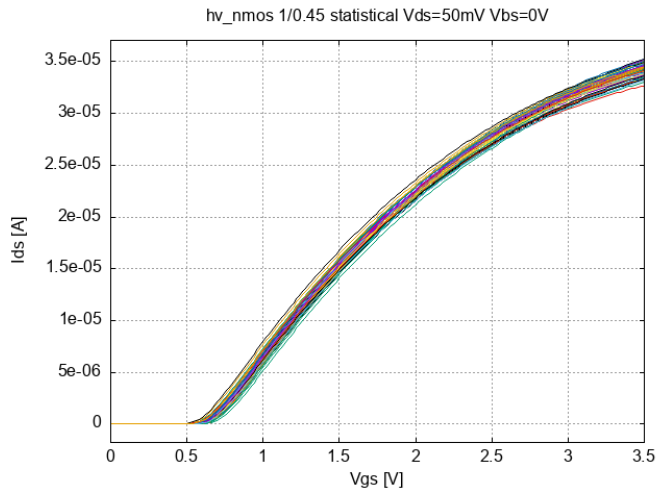
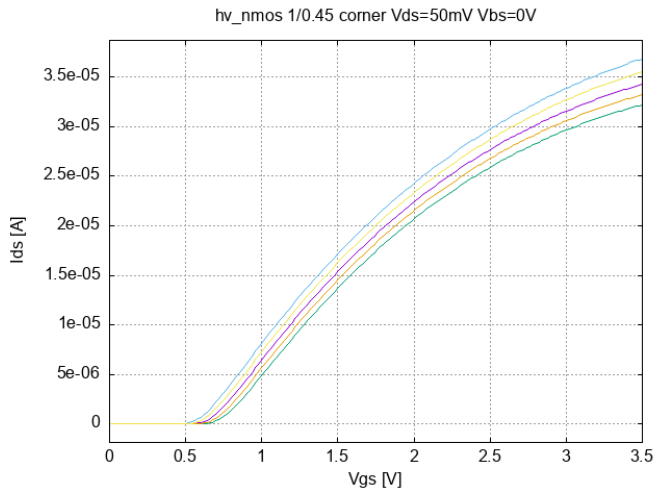
hv_nmos 1/10 mismatch Vgs==1.0...3.0V



hv_pmos 1u/10u



hv_nmos 1u/0.45u



hv_pmos 1u/0.45u

