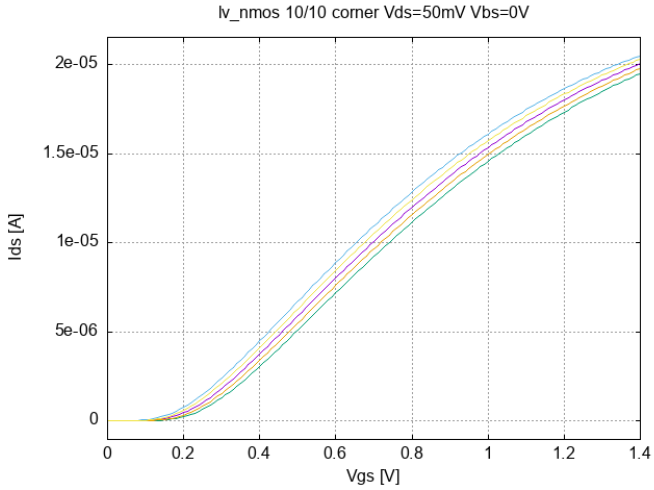
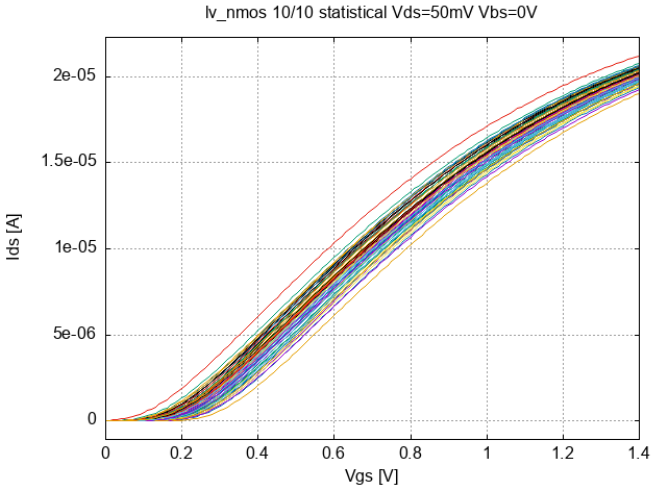
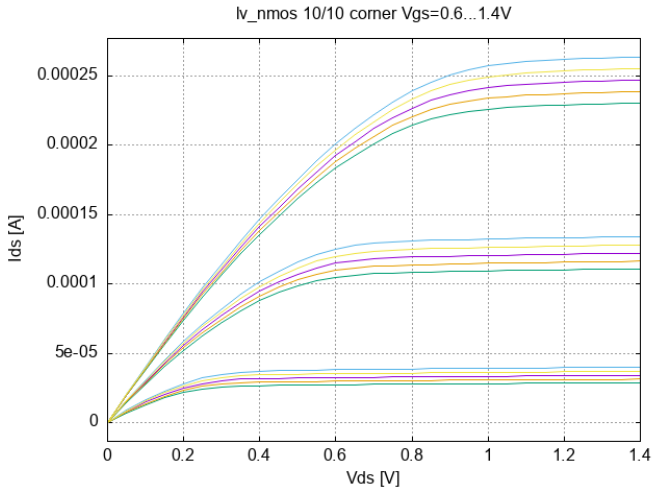
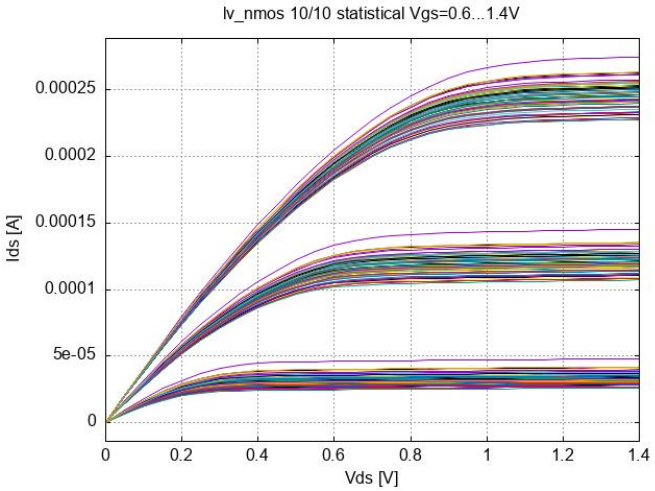
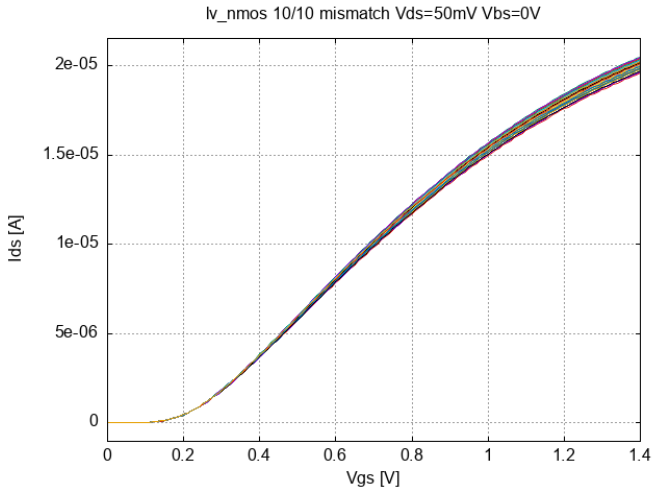
# lv_nmos 10u/10u

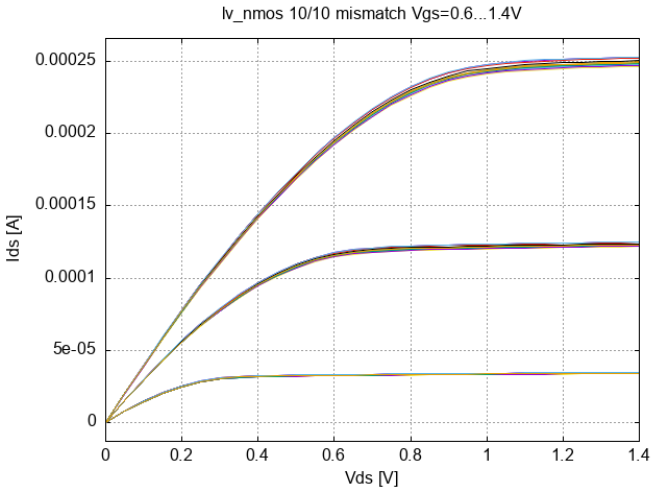


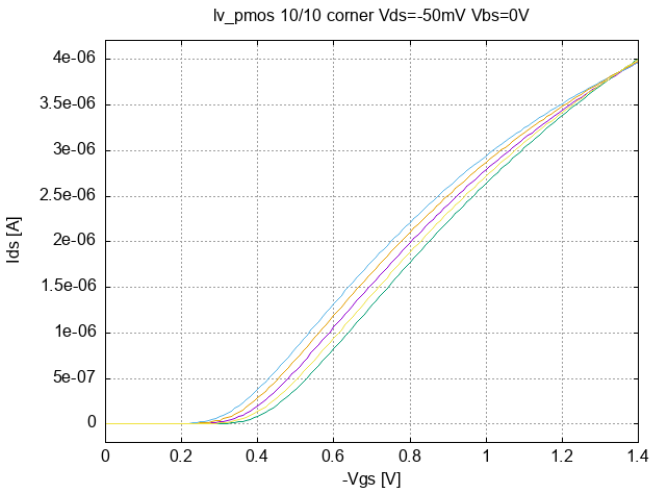



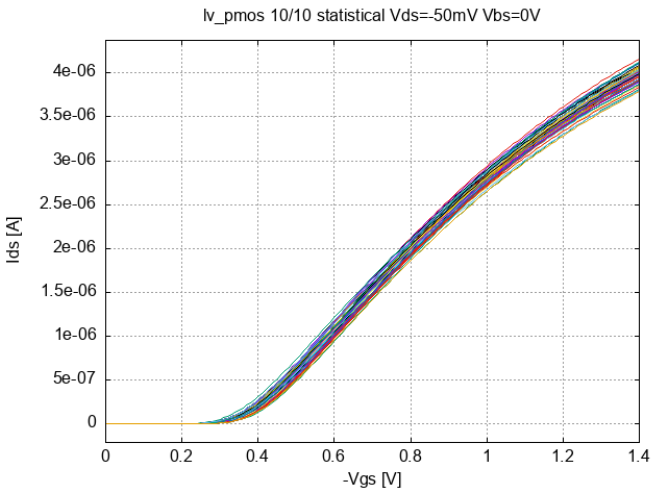



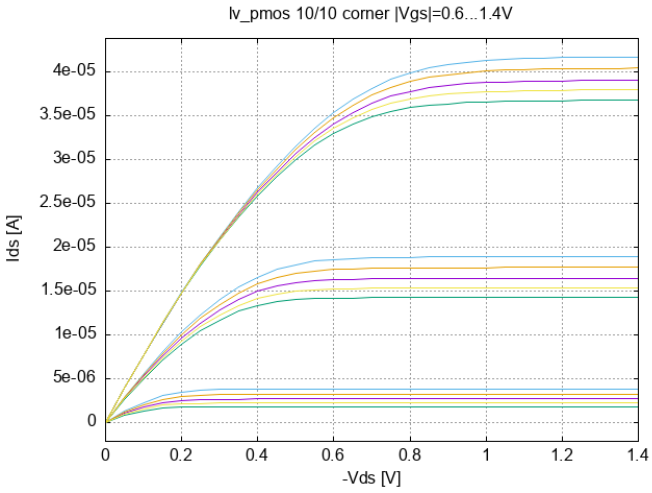



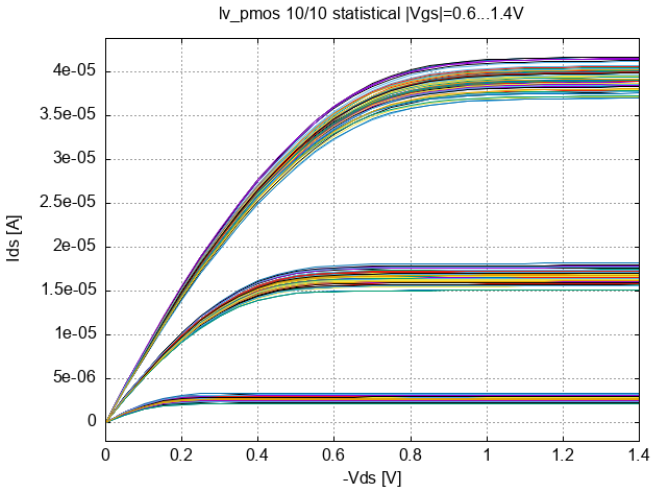



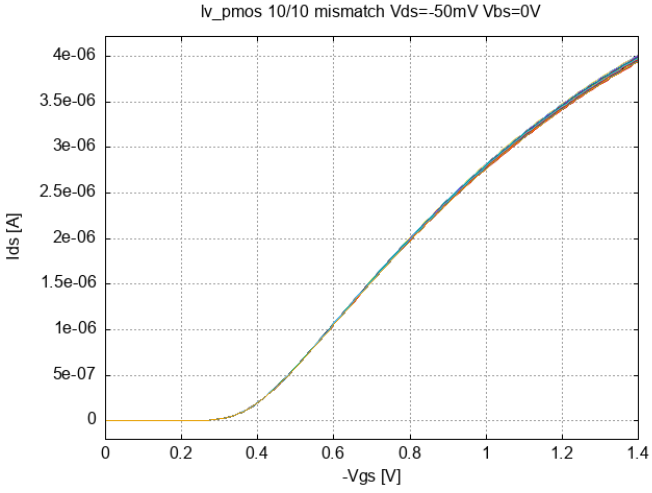
# lv_pmos 10u/10u

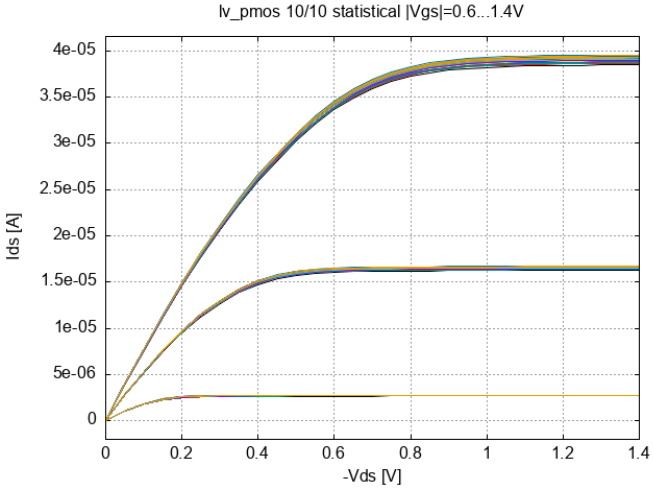


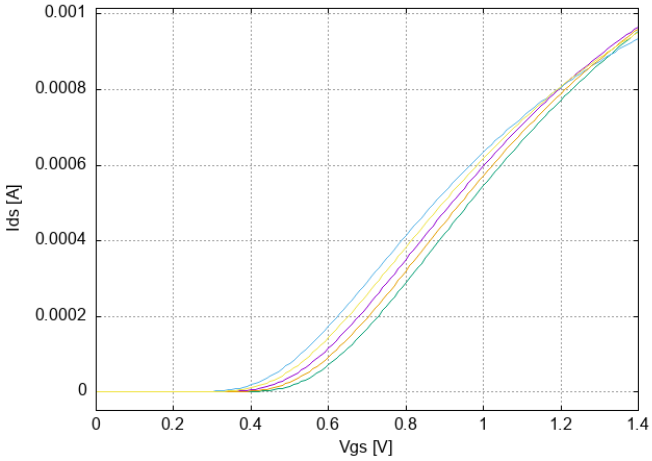



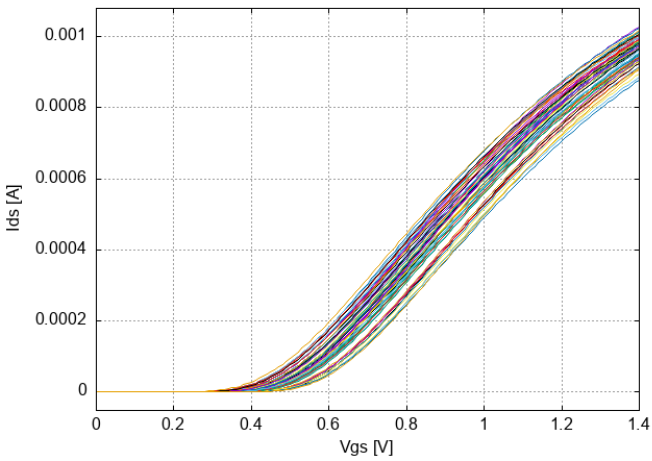



# lv_nmos 10u/0.13u

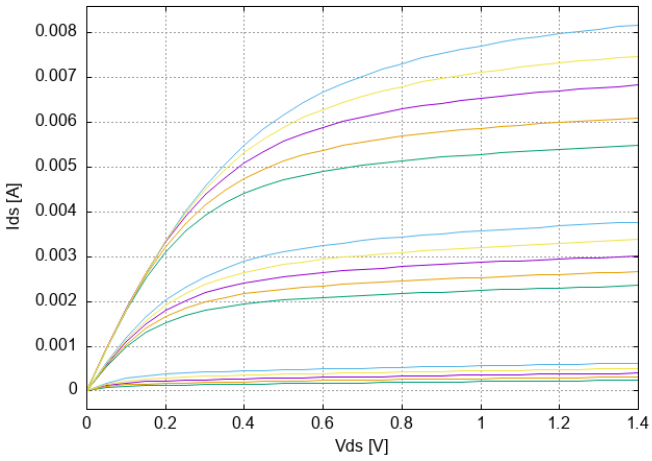
lv_nmos 10/0.13 corner Vds=50mV Vbs=0V



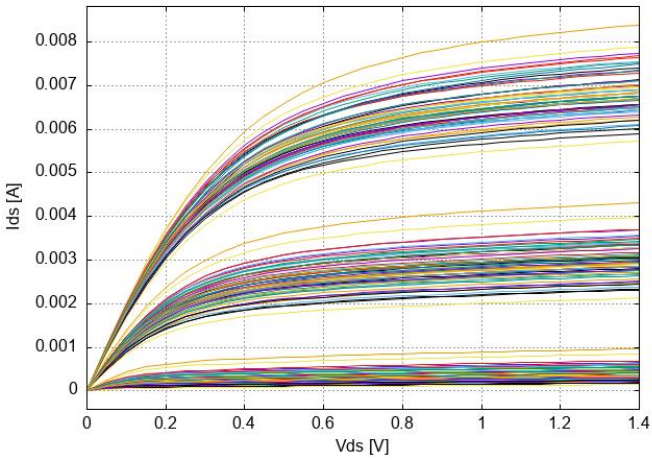

lv_nmos 10/0.13 statistical Vds=50mV Vbs=0V



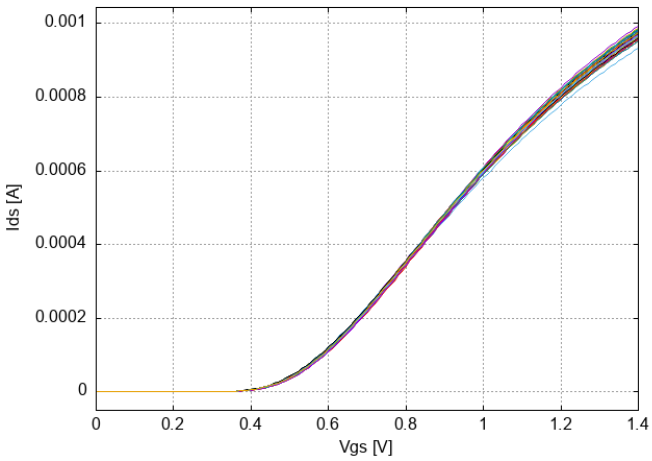

lv_nmos 10/0.13 corner Vgs=0.6...1.4V



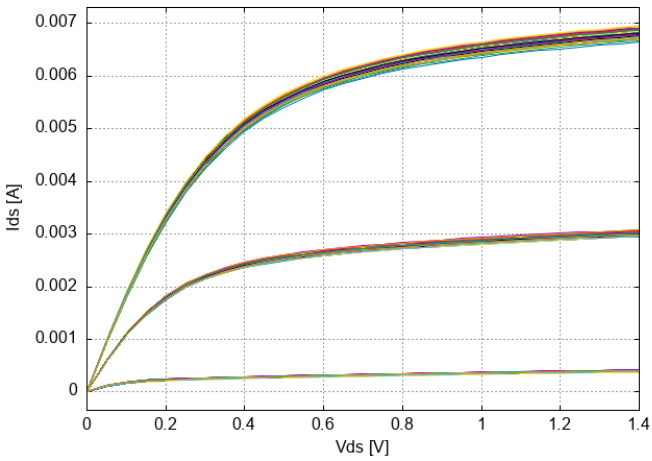

lv_nmos 10/0.13 statistical Vgs=0.6...1.4V




lv_nmos 10/0.13 mismatch Vds=50mV Vbs=0V

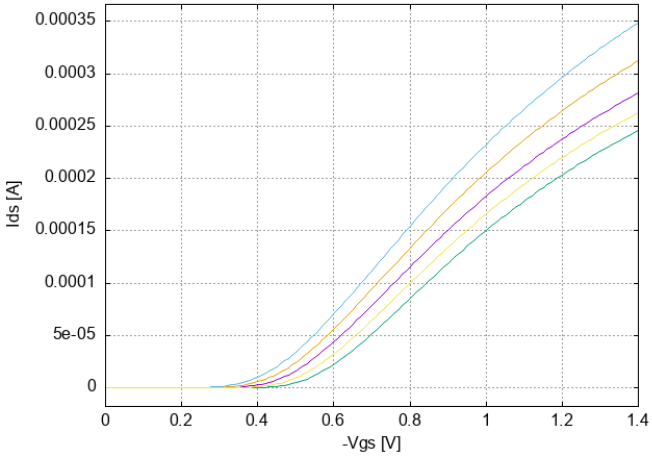



lv_nmos 10/0.13 mismatch Vgs=0.6...1.4V

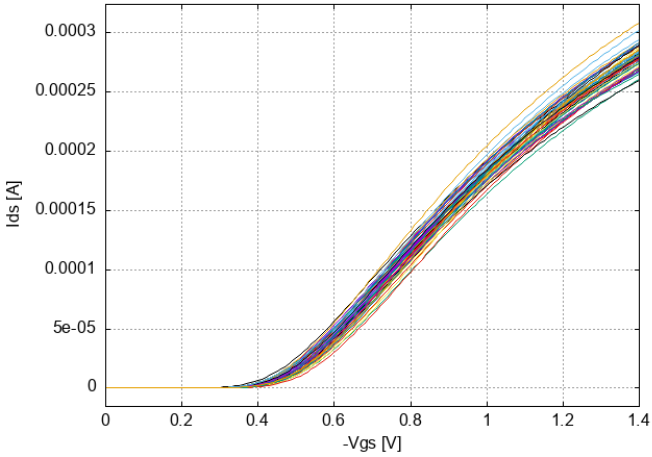


# lv_pmos 10u/0.13u

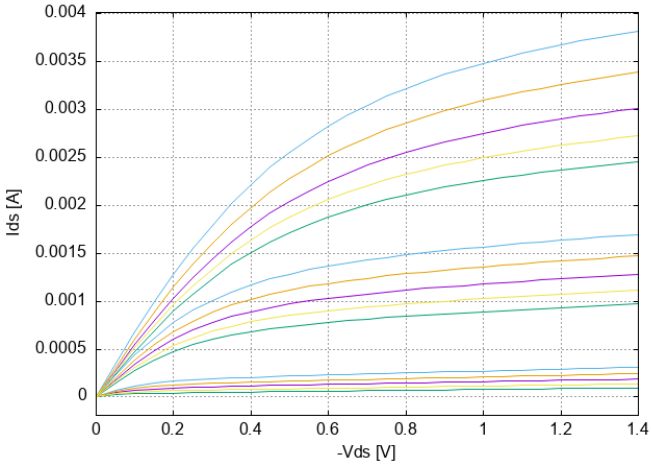
lv_pmos 10/0.13 corner Vds=-50mV Vbs=0V



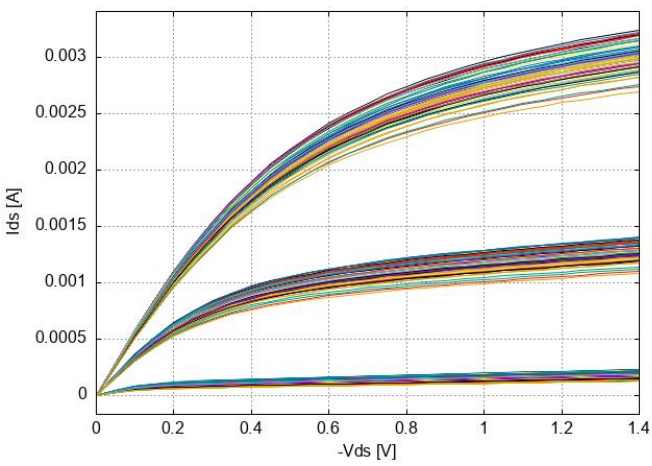

lv_pmos 10/0.13 statistical Vds=-50mV Vbs=0V



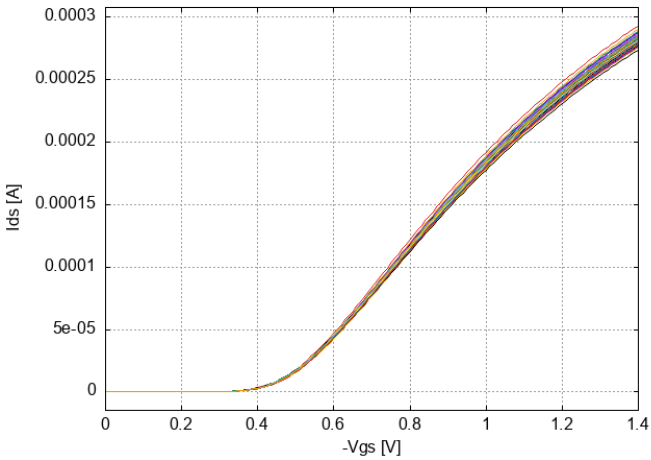

lv_pmos 10/0.13 corner |Vgs|=0.6...1.4V



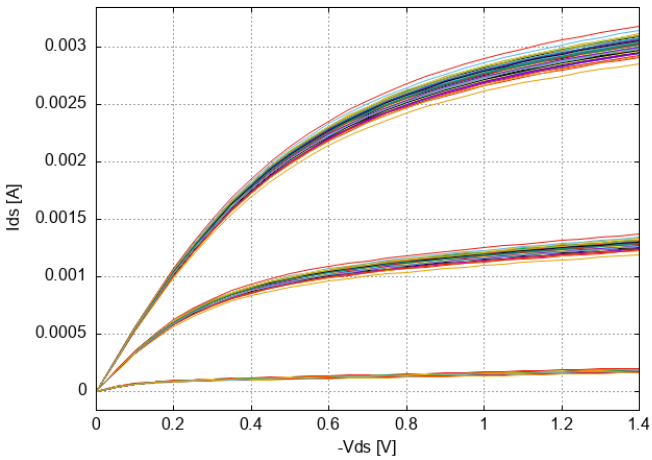

lv_pmos 10/0.13 statistical |Vgs|=0.6...1.4V



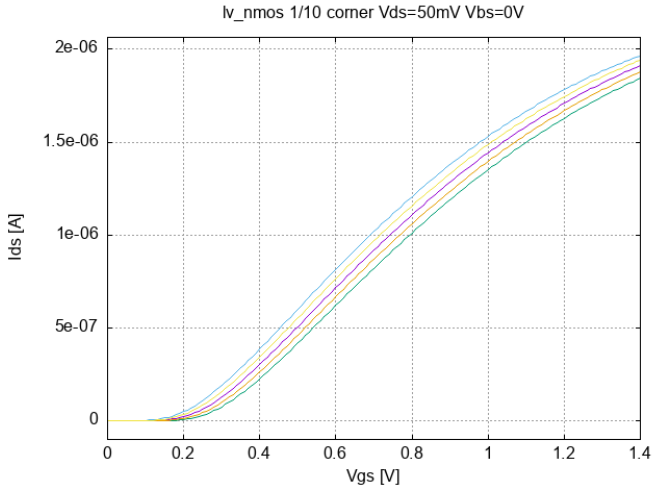

lv_pmos 10/0.13 mismatch Vds=-50mV Vbs=0V

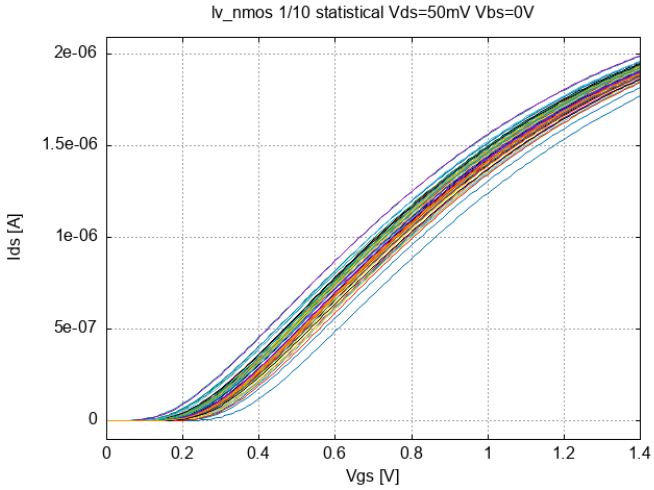


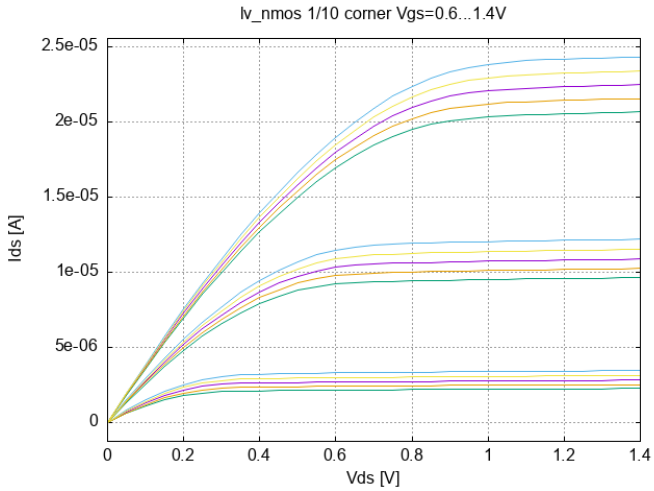

lv_pmos 10/0.13 statistical |Vgs|=0.6...1.4V

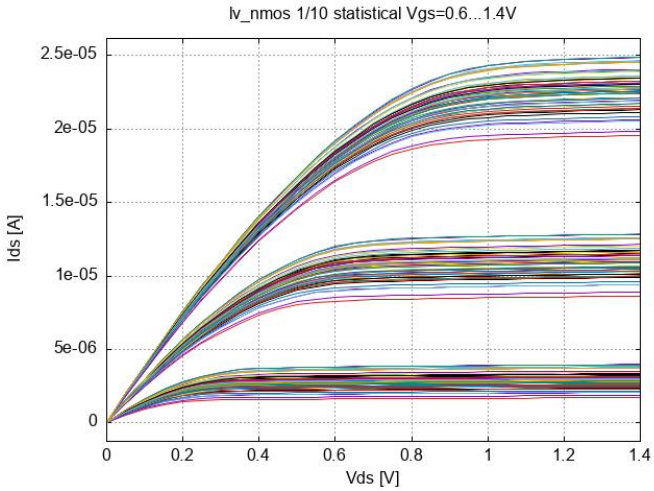


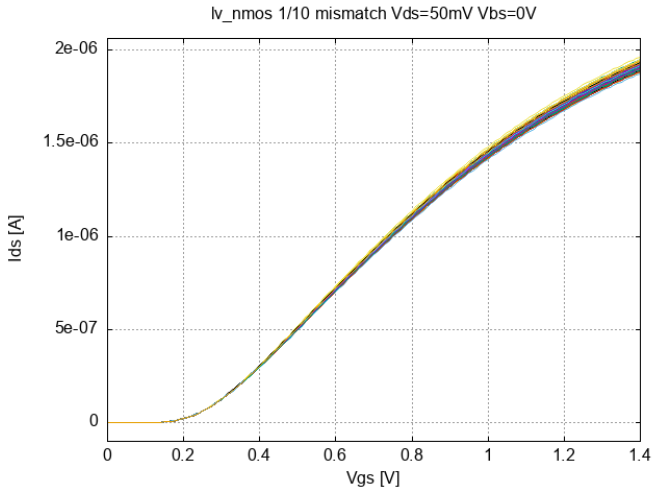
# lv_nmos 1u/10u

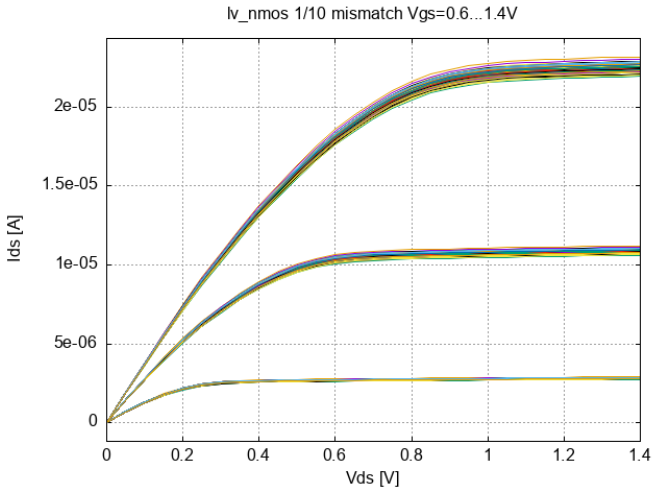


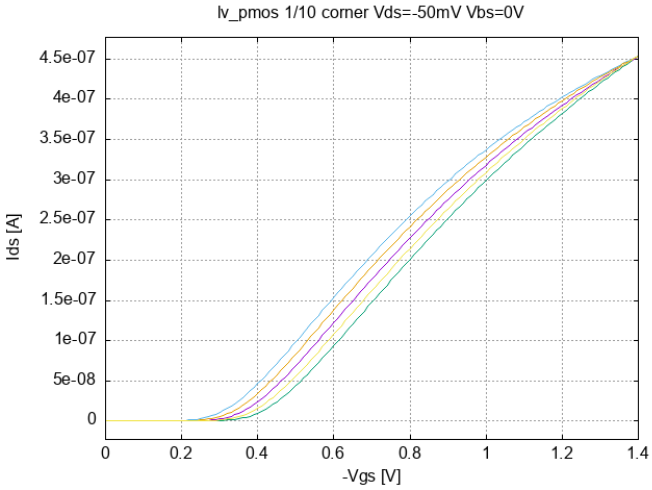



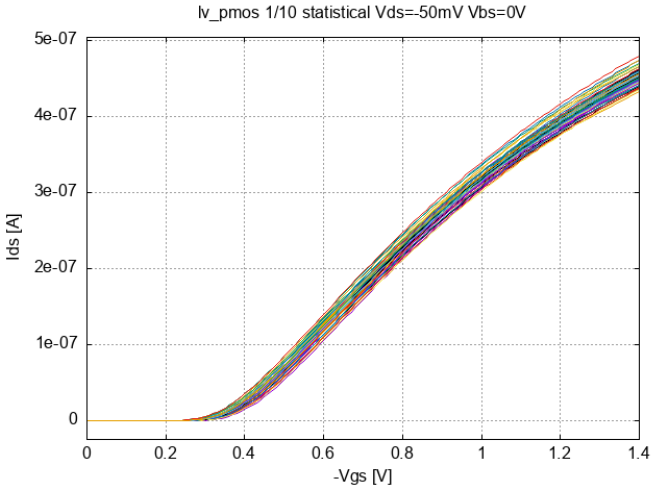



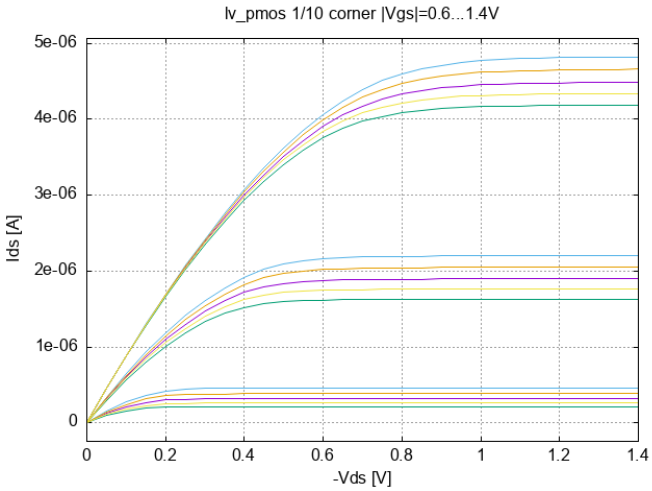



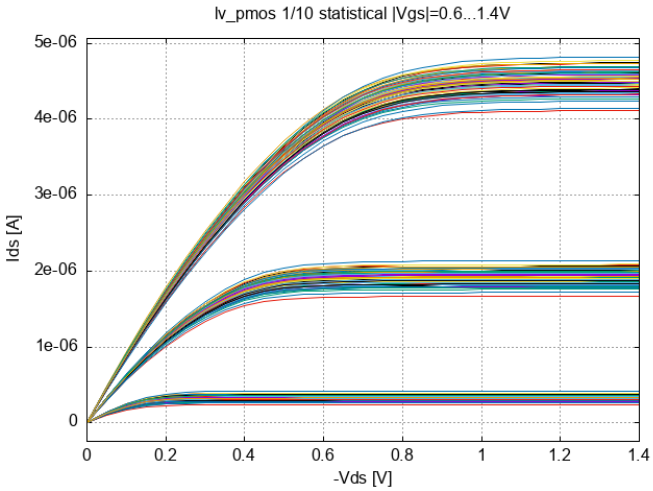



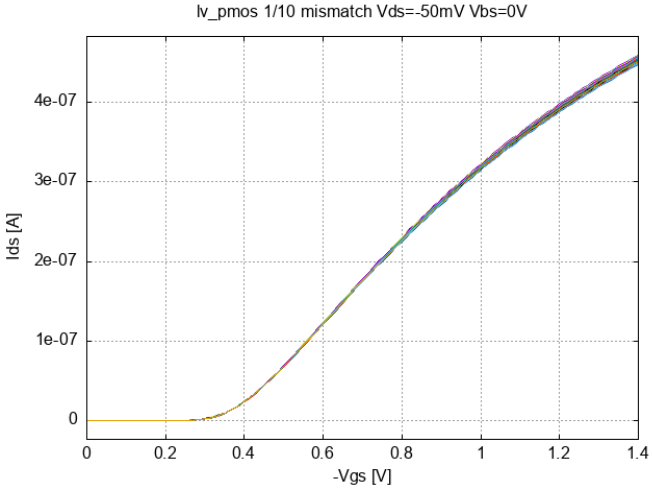
# lv_pmos 1u/10u

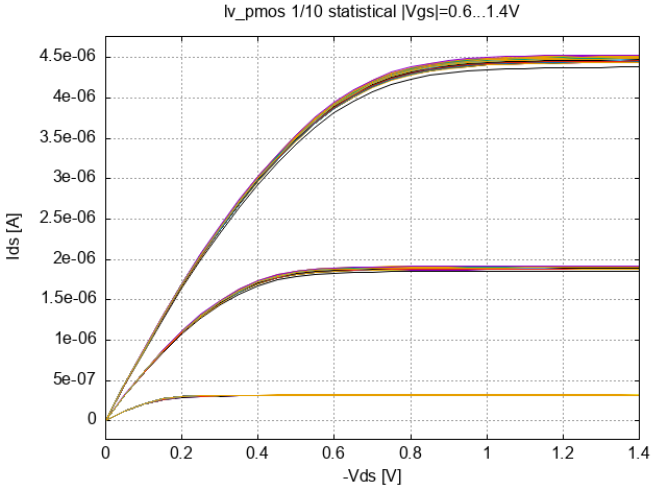


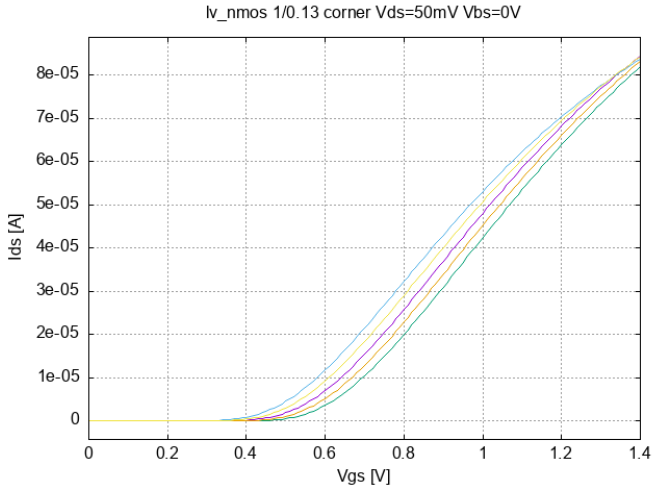



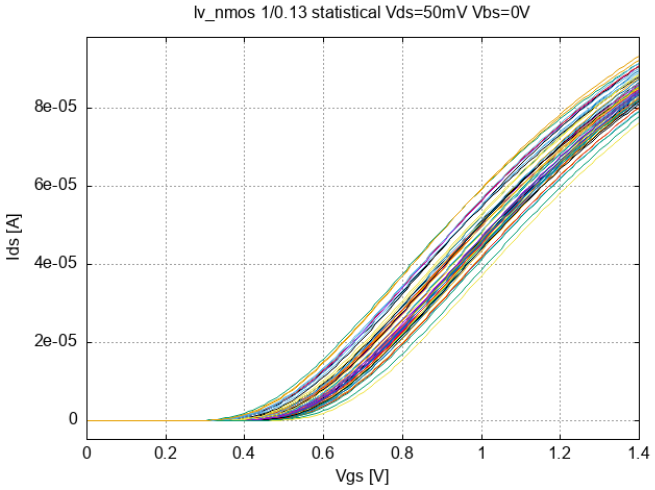



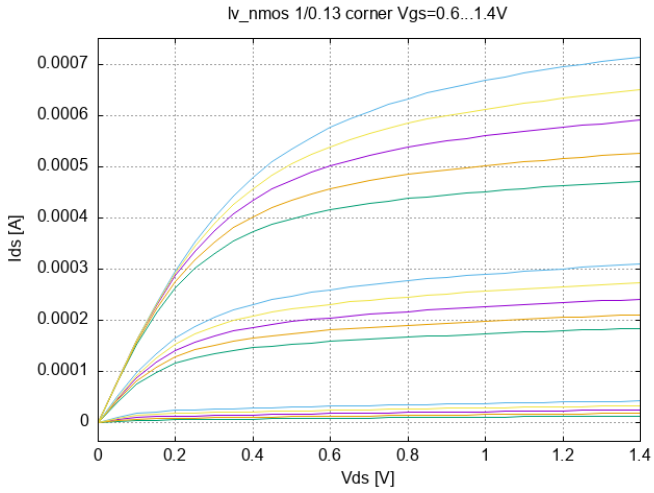



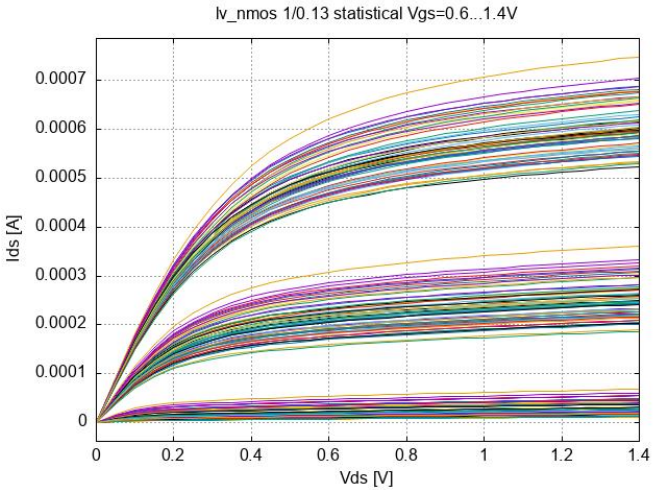



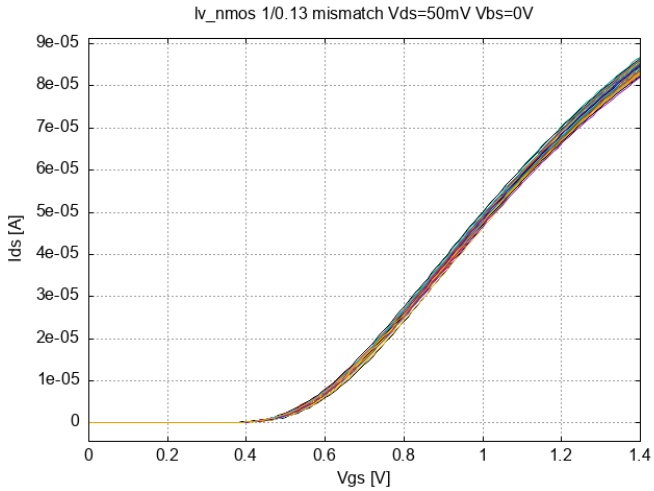
# lv_nmos 1u/0.13u

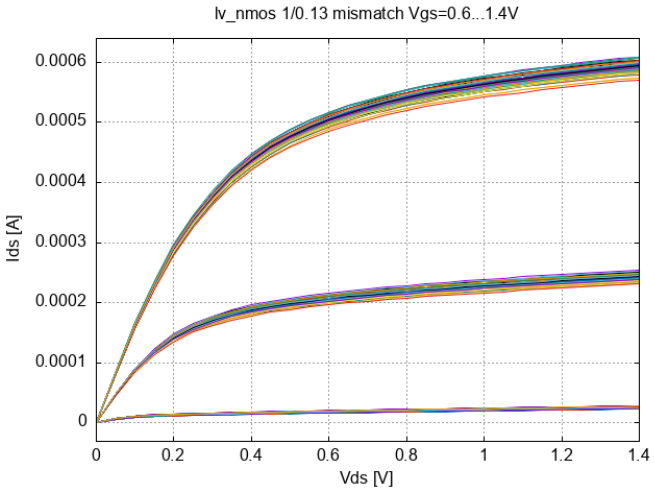


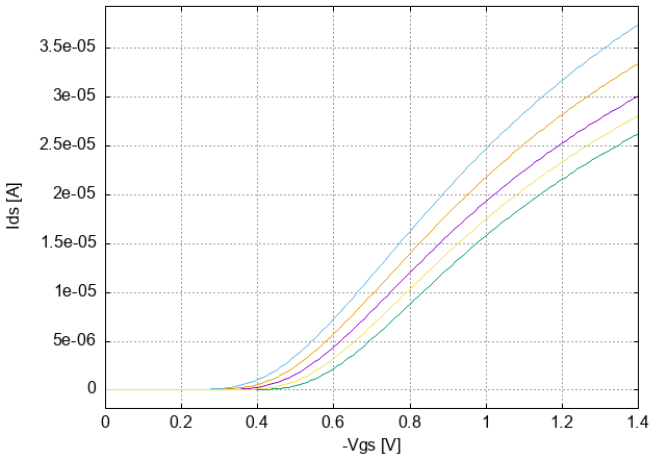



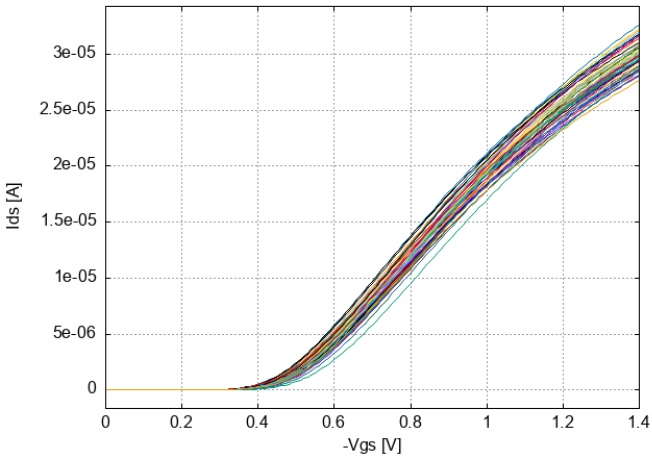



# lv_pmos 1u/0.13u

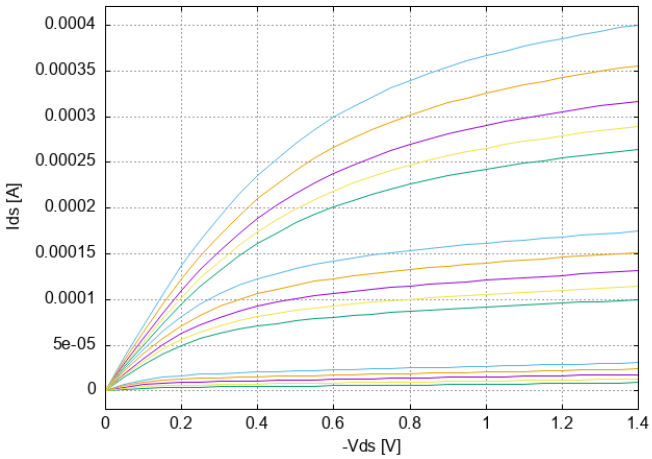
lv_pmos 1/0.13 corner Vds=-50mV Vbs=0V



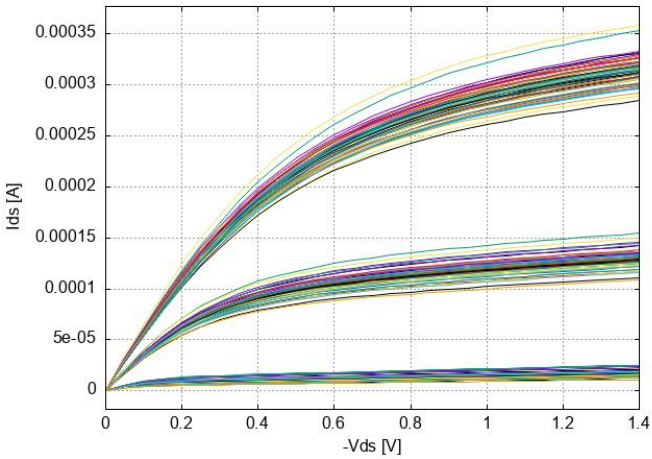

lv_pmos 1/0.13 statistical Vds=-50mV Vbs=0V



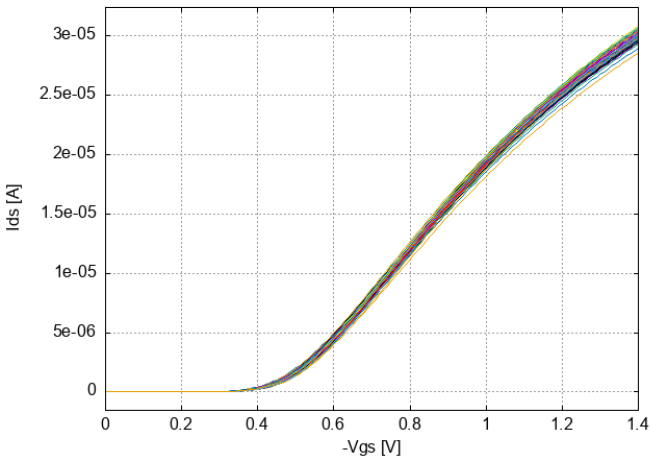

lv_pmos 1/0.13 corner |Vgs|=0.6...1.4V




lv_pmos 1/0.13 statistical |Vgs|=0.6...1.4V




lv_pmos 1/0.13 mismatch Vds=-50mV Vbs=0V




lv_pmos 1/0.13 statistical |Vgs|=0.6...1.4V