ngspice, current status and future developments

Holger Vogt
Duisburg, Germany

ngspice – what is it ?

Circuit simulator that numerically solves equations describing (electronic) circuits made of passive and active devices for (time varying) currents and voltages

Open source successor of venerable spice3f5 from Berkeley

PCB design support

KiCad, Eagle/Fusion360, Altium, PartSim, CoolCAD, WeSpice, Qucs-S, …

Requirements:
Comfortable user interface (offered by third parties)

PSPICE and LTSPICE model compatibility

IC design support

gEDA, Yosys, efabless, Isotel, Google/Skywater PDK, XSCHEM, Google/GF PDK, IHP PDK

Requirements:

BSIM 3, 4, BULK models etc.

Large circuit capability, speed,

HSPICE PDK compatibility

ngspice – where to use it in an analog design flow?

Design specification

- Specifications
- Constraints
- Topologies
- Test bench development

Schematic flow

- System-level schematic entry
- Architecture HDL simulation
- Block HDL specification
- Circuit-level schematic entry
- Circuit simulation and optimization

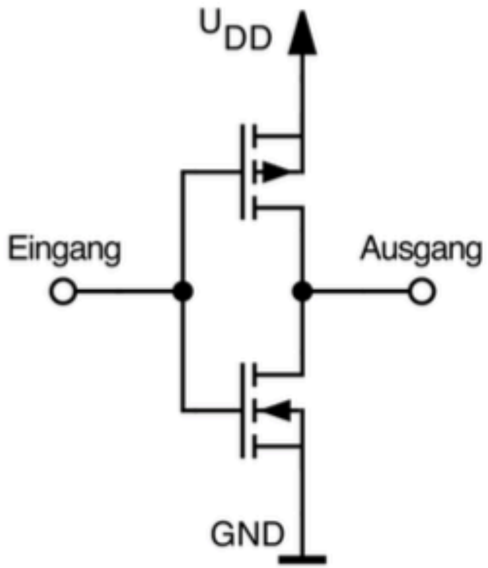
Physical flow

- PCell-based layout entry
- Design rule check (DRC)
- Layout versus schematic (LVS)
- Parasitic extraction
- Post-layout simulation
- Tape-out

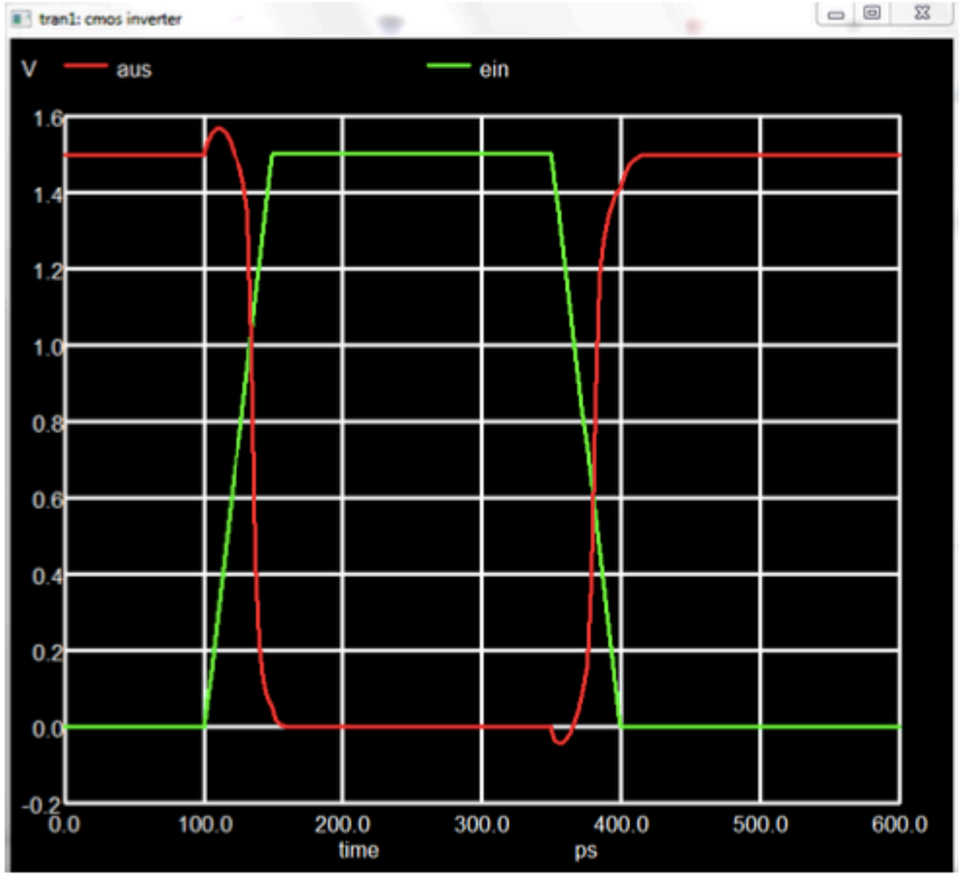
Analog flow:
https://www.allaboutcircuits.com/technical-articles/what-is-analog-ic-design/

open source tools:
https://anysilicon.com/the-ultimate-guide-to-open-source-eda-tools/

Inverter simulation




```
CMOS inverter

.include ./bsim4soi/nmos4p0.mod
.include ./bsim4soi/pmos4p0.mod
.option TEMP=27C

Vpower VD 0 1.5
Vgnd VS 0 0

Vgate Ein VS PULSE(0 1.5 100p 50p 50p 200p 500p)

MN0 Aus Ein VS VS N1 W=10u L=0.18u
MP0 Aus Ein VD VS P1 W=20u L=0.18u

.tran 3p 600ps

.control
  run
  plot Ein Aus
.endc

.END
```

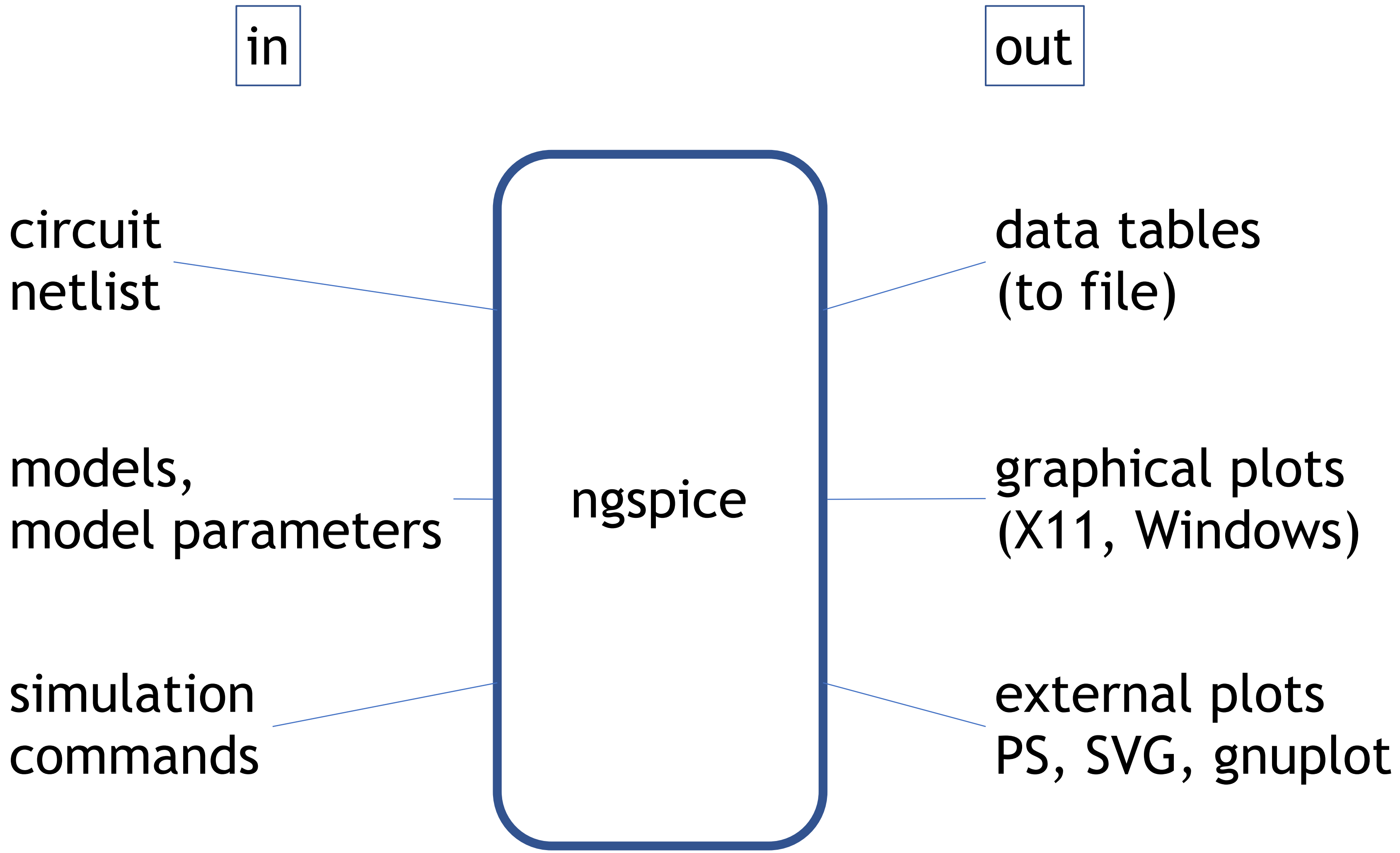


Circuit

Netlist

Transient simulation

ngspice interface



The above is valid for the standard executable. ngspice shared library has a different, data driven API

ngspice device models

Intrinsic models (BSIM3, BSIM4, HICUM2 etc.)

Subcircuit models

Verilog-A compact device models via built-in OSDI interface and OpenVAF compiler, https://openvaf.semimod.de/, model collection at https://github.com/dwarning/VA-Models

XSPICE analog building blocks

XSPICE digital building blocks for fast event-based simulation, auto-interfacing between analog and digital

Behavioral models

Simulations types

Op, dc, ac, transient, small signal noise

Seldom used: pz, tf, distortion

S-parameter extraction

S-parameter black box ac simulation (using S2SPICE, under test)

Monte-Carlo (using internal scripting language)

ngspice internals

C, C++ code base, compiles on all operating systems

X11 or native Windows graphics interface

Sparse matrix solver, optional KLU matrix solver currently under test
(KLU runs with a 200k transistor circuit, Skywater PDK)

ngspice is available as a shared library (ngspice.dll or libngspice.so).
The API allows very detailed control of many simulator parameters.
The calling program handles all I/O.

Scripting language to run parameter sweeps, Monte-Carlo, or others

Third party integration into Python (at least three sources)

Support and QA

Support:

discussion forums (fast response, typ. < 24h)
mailing lists

Quality assurance:

make check runs and verifies basic circuits and models (BSIM3, 4, HiCUM and others).
Paranoia test suite run a script with about 40 circuits of all kind.

ngspice and IHP-Open-PDK

Bipolar transistors

- VBIC model enhanced (SOA parameters added)
- VBIC model tested with PDK parameters

Resistors

- R3_CMC model (Verilog-A) for non-linear semiconductor resistors compiled with OpenVAF and tested with ngspice

MOS transistors

- PSP 103.8 model (Verilog-A) compiled with OpenVAF, tested with standard parameters (IHP parameters not yet available)

ngspice, to be done

Integration support

PDK IHP

Any new interfaces?

Finalize KLU integration

Finalize OpenVAF/OSDI (e.g. noise support)

Update Sparse matrix solver

Tentative:

Compound element pseudo transient analysis method

(improve dc operating point evaluation)

Integration of digital event based simulation into design flow

(Verilog to XSPICE?)

More RF support (S-parameters, HB …)