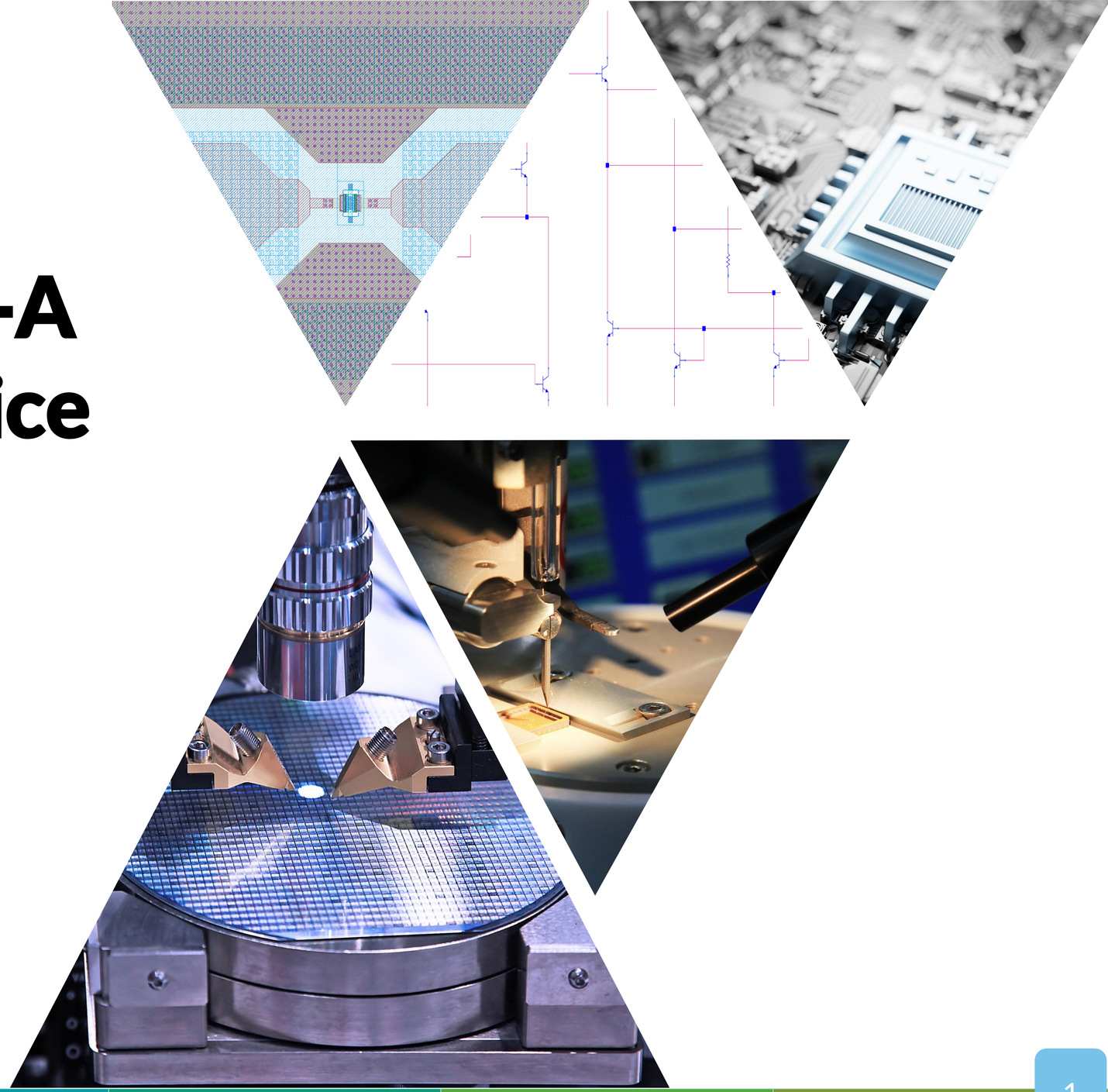
OpenVAF – Next Generation Verilog-A Compiler with ngspice integration

Markus Müller

SemiMod

www.semimod.de



Outline

- What is a compact model?
- Why Verilog-A?
- Introduction to OpenVAF
- Outlook
- SemiMod Company Overview

What is a compact model?

- A compact model allows predicting a semiconductor device's ***terminal characteristics*** as functions of ***bias, geometry, and temperature***.

- The model must be “adjusted” to each technology using a process called ***model parameter extraction***

- There are ***different*** compact models:
  - physics-based vs. empirical models
  - analytical vs. data-driven models
  - small-signal vs. large-signal models
  - for every different type of semiconductor device
  - different model versions

- Models are complicated pieces of numerical code

Compact Model Coalition

Industry Cost-Savings through Standard Models

Why Verilog-A? (1)

- Circuit simulation requires ***sufficiently accurate models*** of devices
- ***Consequences*** of bad models:
  - measured circuit characteristics ***not as simulated***
  - possibly ***expensive*** iterative tape-outs to reach spec.
  - circuit simulation **run-time/convergence** bad

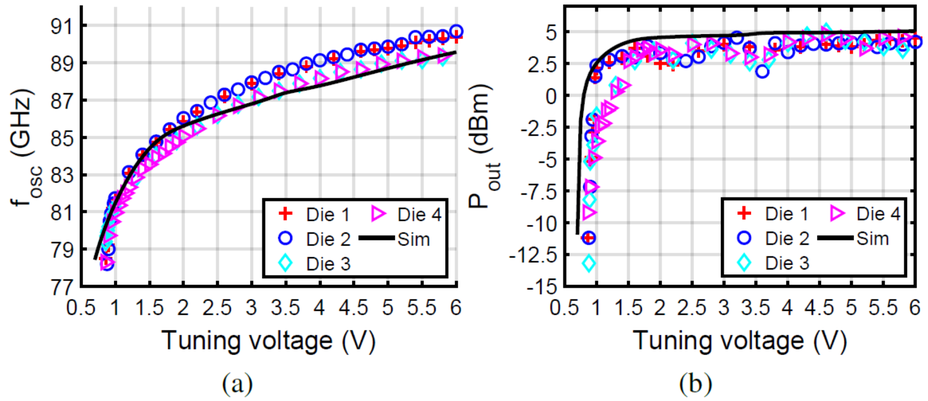
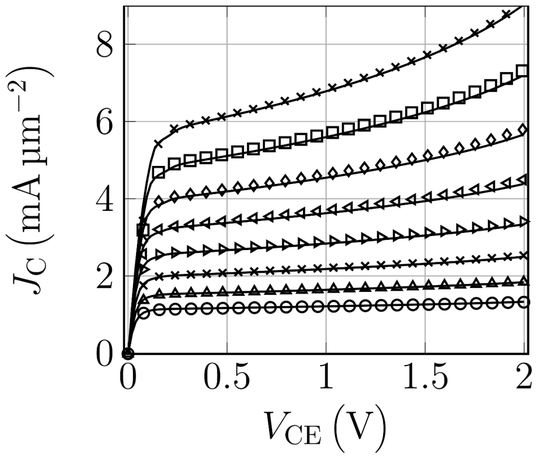
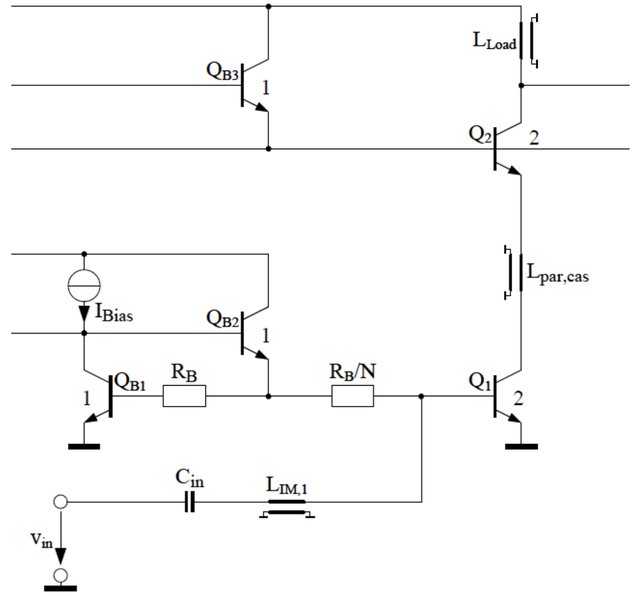


Fig. 5. Measured and simulated (a) oscillation frequency and (b) output power as a function of the tuning voltage for 4 different dies.

Results for oscillator with SemiMod model



Results for npn output characteristics.



Schematic = connection of many devices, each need model

Without a quality model:

$\Rightarrow$ Circuit designer's work becomes ***"black magic" and frustrating***

$\Rightarrow$ Possibly ***enormous follow-up costs necessary*** due to re-design and debugging

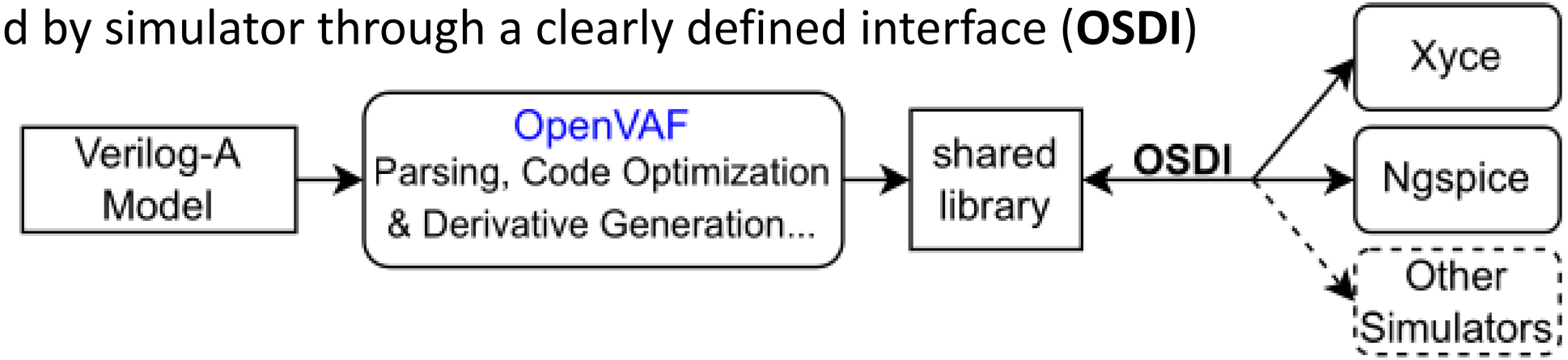
Why Verilog-A? (2)

- **Open Source Gap**: simulators **do not implement many compact models**
  - Missing models in ngspice: FinFET (BSIM-CMG), FDSOI (BSIM-IMG, LT-UTSOI)
  - Model **implementations needed** to enable analog simulation
  - Model implementation is **time and knowledge-intensive**

=> Serious show-stopper for open-source PDKs

=> Models are released as Verilog-A source files

- **Solution**:
  - Verilog-A compiler that generates machine code from a given **Verilog-A** model code
  - Interfaced by simulator through a clearly defined interface (**OSDI**)



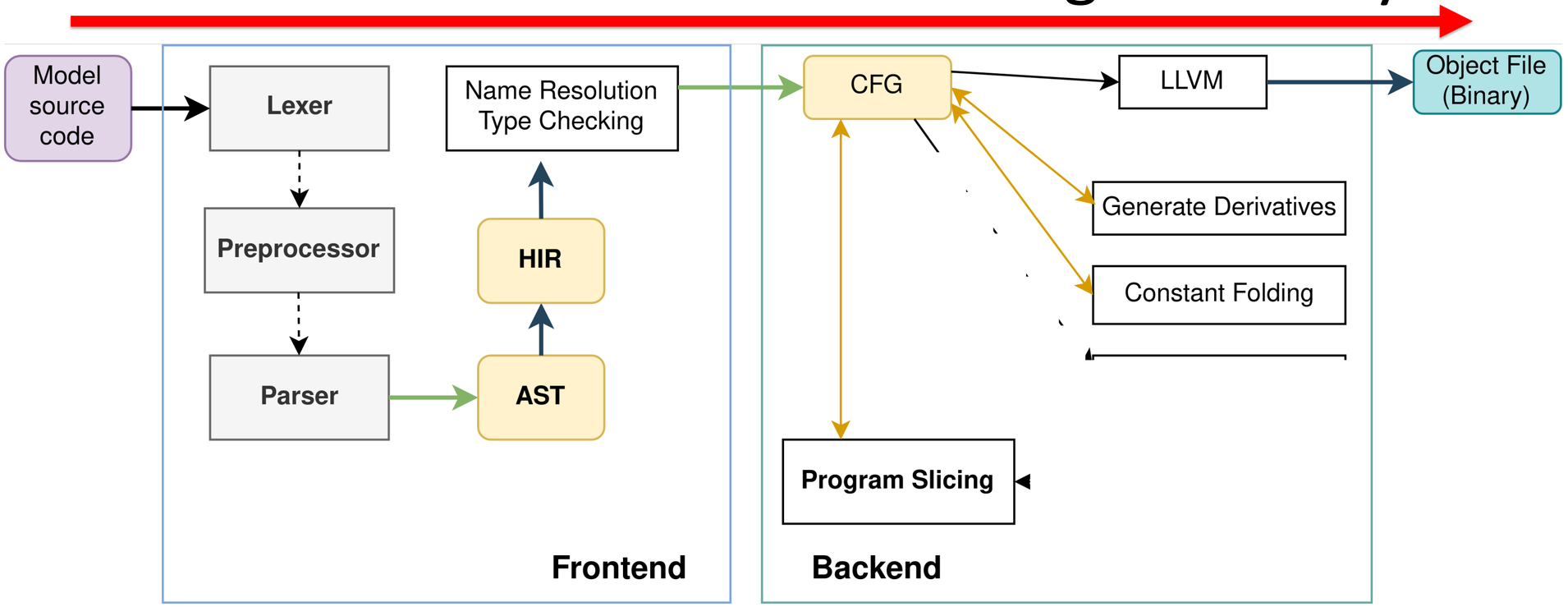
Introduction to OpenVAF (1)

- OpenVAF is a Verilog-A compiler that …
  - … directly generates executable ***machine code***
  - … offers ***fast compilation*** without the need for another compiler (gcc)
  - … implements the language standard in a ***clear and unified*** way
  - … has **great ux** (error messages)
  - … is ***open source and licensed under GPL***
  - **… is fully integrated into ngspice**
- Business model:
  - commercial partners can request commercial license, software integration services into circuit simulators and support
  - can leverage ngspice for parameter extraction, no commercial license required

Introduction to OpenVAF (2)

- design inspired by modern compilers (clang, rustc, swift compiler)
- full name resolution and type checking
- focus on helpful error messages
- Back-end: state of the art algorithms to support efficient code generation
- directly generate shared objects -> can load model at runtime

from Verilog-A directly to binary



Introduction to OpenVAF (3)

- Usage:
  - Download and install ngspice from https://sourceforge.net/projects/ngspice/
  - Download and install OpenVAF from https://openvaf.semimod.de/
  - Compile Verilog-A model with OpenVAF in terminal

```
openvaf hicumL2V3p0p0.va
```

  - Put path to model into ngspice netlist

```
VB B  0 DC 0.1 AC 1 SIN (0.5 0.4 1M)
VC C  0 DC 1

.model npn_full_sh hicuml2va
.include model.l

N1 C B 0 0 npn_full_sh

.control
pre_osdi hicumL2V3p0p0.osdi
```

- Problems?
  - Git repo with issue tracker
  - Ask us for help

Introduction to OpenVAF (4)

- **Enables open-source PDKs** that use models not available in ngspice
- Development so far **privately funded by SemiMod**
- Widely **recognized** in the open-source EDA community (Other Git projects, issues, mails etc., other simulators like SpiceOpus)
- Used at SemiMod **every day**

Introduction to OpenVAF (5)

- OpenVAF **outperforms** even commercial tools in some aspects
- Models compiled with OpenVAF **have comparable convergence and evaluation speed to built-in models**

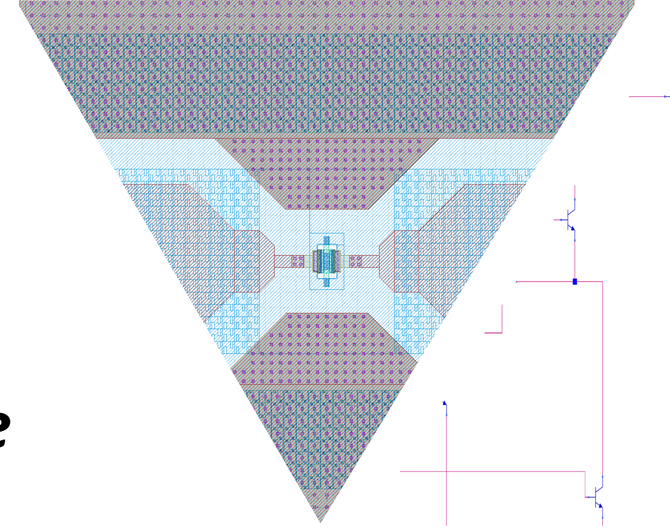
Model compilation time comparison:

	PSPv103	BSIM4	EKV2.6	JUNCAP200
OpenVAF	3.48	6.7	0.23	0.61
Xyce ADMS	109	25.1	9.6*	16.6
ADS	33.9	27.0	2.5	5.1
Spectre	27.4	-	6.1	11.4

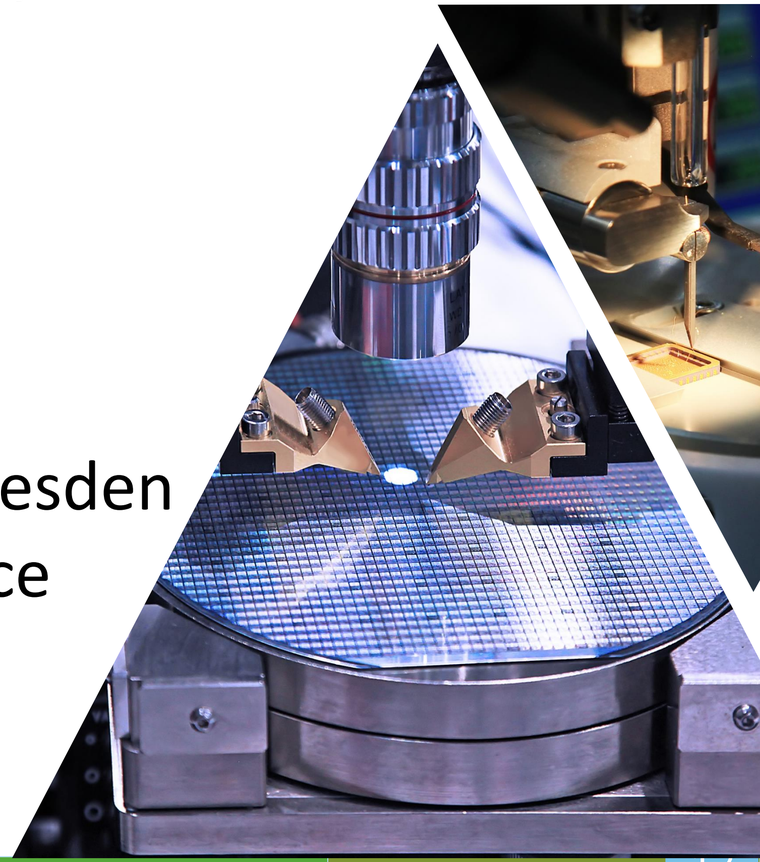
Outlook

- **Noise simulation** not yet implemented (applied for funding)
- **Developer community** too small!
- Covers only **a subset of Verilog-A** used by CMC standard models
- Integration into other simulators beneficial (Xyce)
- Long-term funding not yet achieved

SemiMod - Company Overview



- SemiMod provides
  - ***…device modeling , characterization*** and ***test structure layout design*** services to the semiconductor industry
  - …custom ***software development*** services
- SemiMod is
  - …a ***start-up company*** founded in 2021
  - …specialized in ***Heterostructure Bipolar Transistor*** modeling and characterization
  - …has an ***experienced team*** of engineers from TU Dresden
- SemiMod has ***extensive experience*** with cryogenic device modeling due to prior projects



Discussion/Remarks

- Which compact models are you interested in?
- Is there interest in Neural-Network models?
- We are looking for **partners** for MOSFET parameter extraction tool project!

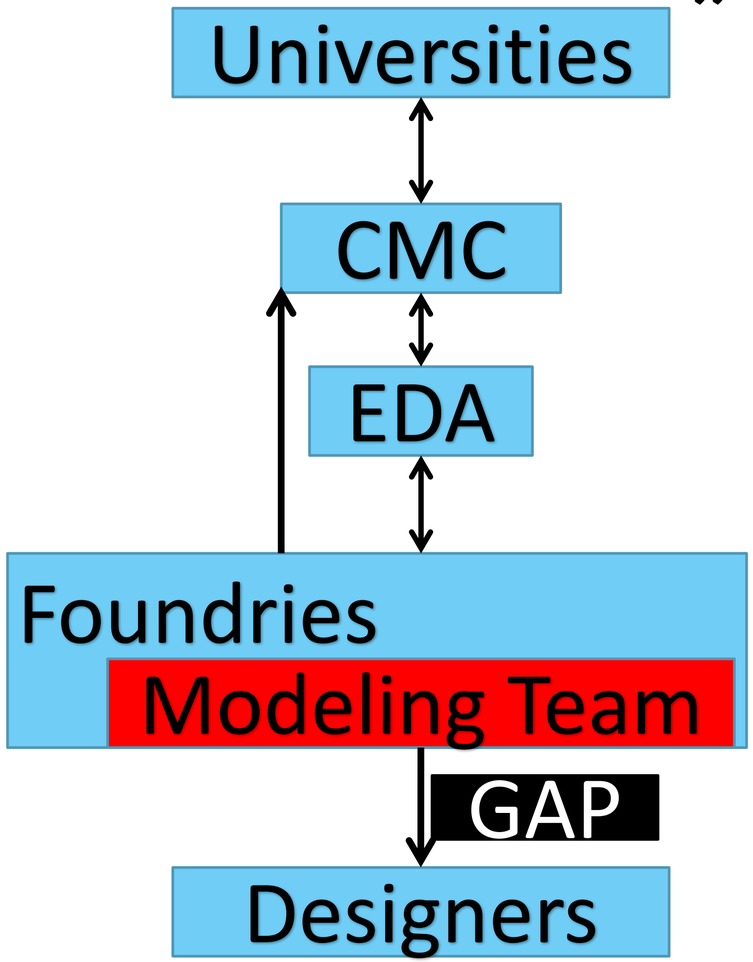
  We **have funding**, but need a **test chip and measurements**, ideally for IHP technology

Thank you for listening!

Special thanks for H. Vogt, R. Scholz,

M. Schröter, NLnet Foundation

„The Gap“ (1)



Simplified as-is structure depicting the way from model to designer.

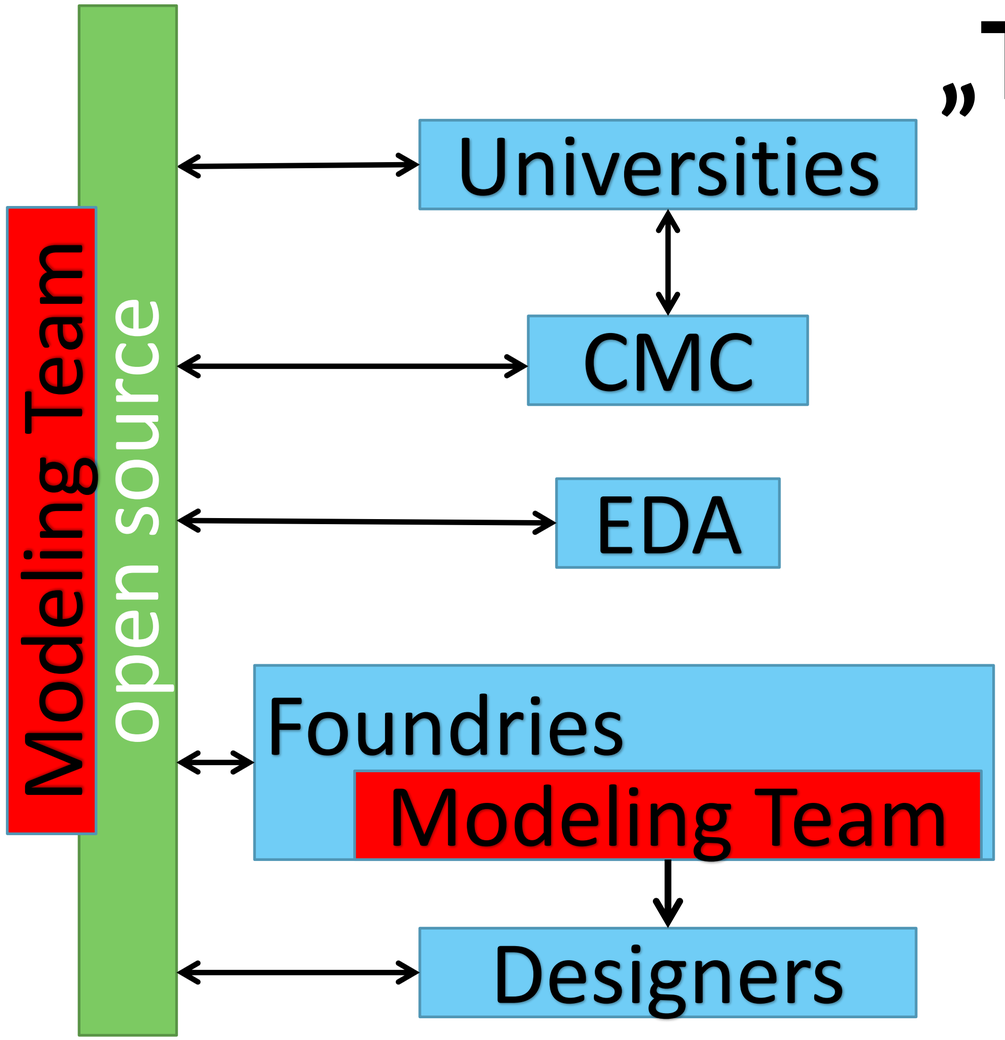
- Universities develop compact models
- CMC standardizes models
- EDA companies integrate models and supply software
- Designers receive models as part of PDK

Problems:

- not much ***communication*** between modeling and design
- Who is ***responsible*** for “the model”, what is the model??
- Models are ***not questioned***/accepted as-is

Can we do better?

„The Gap“ (2)



Simplified as-is structure depicting the way from model to designer.

- we can adopt ***a software mindset*** when it comes to modeling
- Models and PDKs as ***“Git” projects***
- Slack and Git as a ***communication*** vehicle between modeling and designers
- ***Open-source*** software to enable everyone to handle models
- ***Modeling team with direct communication to designers***