Introduction FMD-QNC project status and IHP OpenPDK Roadmap

René Scholz – Group Leader Research & Prototyping Service

Leibniz Institute for high performance microelectronics

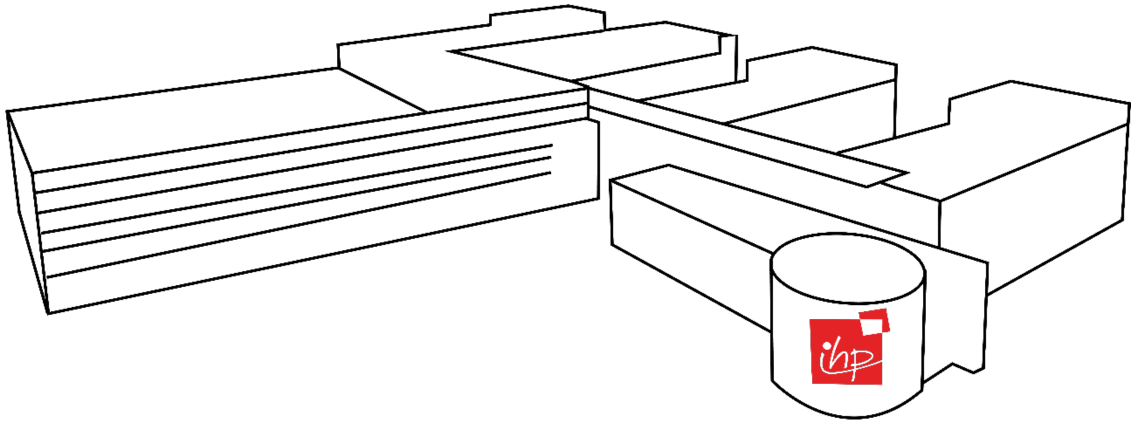
Networking Workshop FMD-QNC OpenPDK, OpenTooling and Open Source Design – An Initiative to Push Development

27th /28th June 2023

IHP Overview

Our position

- IHP is a **European research and innovation center** for silicon-based systems, radio frequency circuits and technologies.
- Research focuses on **socially relevant topics such as communications, mobility, health & environment, industry & agriculture, sustainability and security**
- With its research programs, the IHP makes an important contribution to the **technological sovereignty of Germany and Europe**



IHP Overview

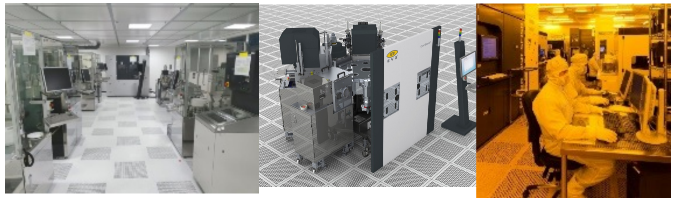
Profile and strenghts

- **Vertical research concept** from **materials research and technology to circuits and systems**
- International leadership and visibility in all of its research areas
- Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated **under industry-oriented conditions, 24/7**, for the provision of **prototypes and small batches**
- **Qualified technological platform** with direct access for science and industry

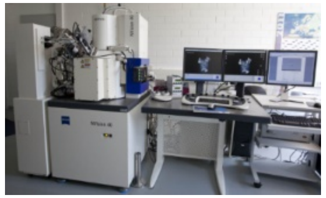
Research & Service in Technology Department

Infrastructure

24/7 operation of 8" Pilot Lines for 130nm SiGe-BiCMOS / EPIC

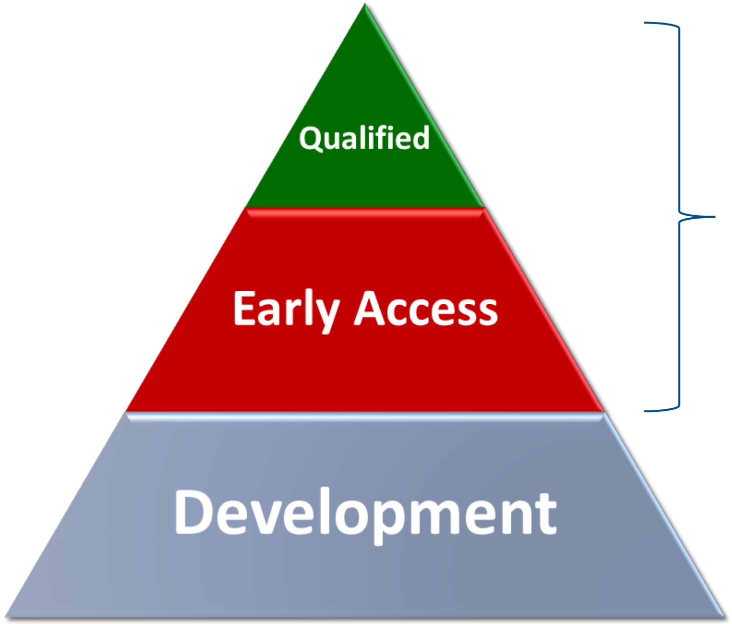


8" wafer bonding (temporary, permanent, µTP,..)



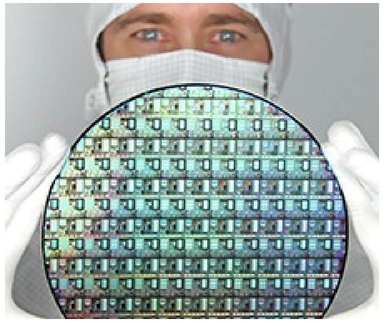
Metrology & mmW, THz e/o char.

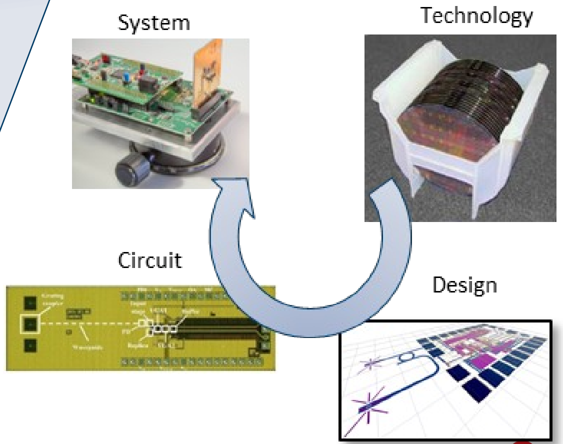
Technology platforms



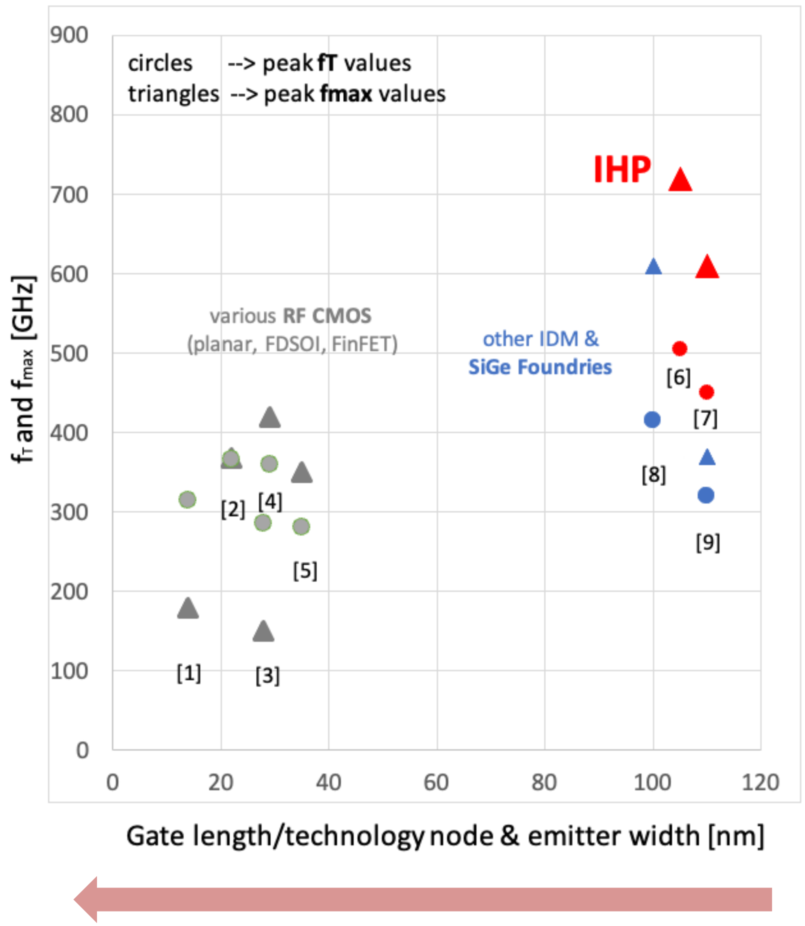
Service

MPW prototyping & LVP





SiGe Heterojunction Bipolar Transistor and BiCMOS



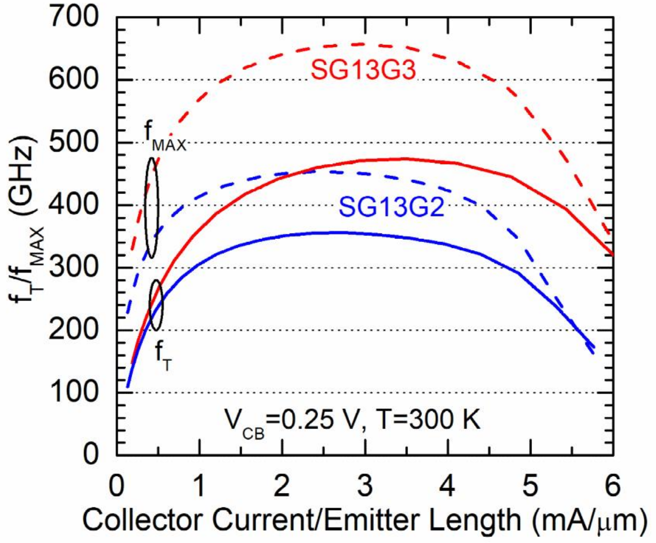
Technology complexity increase

- SiGe BiCMOS targets frequencies and data rates which are out of reach for state-of-the-art CMOS ➔ physical limitations for RF-CMOS
- Compact and highly scalable technology
- Cut-off frequencies (f_T, f_{max}) are
  - Up to 2x higher for SiGe BiCMOS at lower process complexity
  - Typically 3-10x larger than operating frequency
    - ➢ **+100 GHz application as 6G, D-band communication, radar etc. require SiGe RF technology as a scalable manufacturing technology**

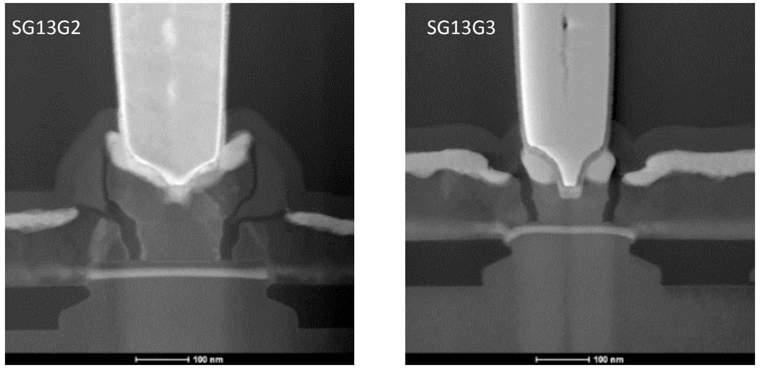
Evolution of High Performance BiCMOS Technologies

	SG13S	SG13G2	SG13G3
HBT f_t / f_{max}	250 / 340 GHz	350 / 500 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

*Cu BEOL from X FAB



f_t and f_{max} of IHP SG13G2 and SG13G3 technology



TEM cross section of an HBT with elevated extrinsic base regions from (a) the SG13G2 process and (b) a t SG13G3 HBT

- SG13G2 technology was selected for the development of an open source PDK

Motivation for IHP's open source PDK initiative

- Provide low threshold access to technology & design data, PDK and design tools for chip designer, technology developer & academic projects
- Simplify access to education material for chip designer
- Initiate cooperation's and joint projects with open source community
- Support chip design possibilities for small design projects
- Pipe cleaner to demonstrate possibilities and convince commercial fabs to support open source approach

IHP / Open Source in FMD-QNC project

Push Microelectronic Academy –
Certified Design Courses & Design Infrastucture

Develop Open-Design-Plattform / Tooling & PDK

Support with Free Area in MPW Runs

Microelectronic Academy - Focus on open source tools

- Develop an certified digital Design course (certified) – starting 2023
- With with first version of open PDK – training on technology, open PDK, open Tools with simple digital and analog design example
- Later (2024, 2025) use RF Design examples (from CoreExpert Group) to develop extend PDK analog design training course
- Schedule training runs 2024 – 2026 (together with Europractice)

Central Design-Infrastructure for open Tools

- 2023 Start with test server for existing open tools and PDK (Skywater)
- 2024 Small open cloud server to improve and test open source Tools and IHP PDK
- Use open cloud server for training pilots
- Evaluate Cloud system & container solutions for education and design tasks

Open PDK & open Tool Development

- This provides bases for education of designer and design projects
- IHP started on existing experiences of “Skywater project”
- IHP will dig more in analog design flow later RF design (details in next talk)
- Quality should fulfill requirements for academic education
- Tools must be improved, interface development is crucial

- For a sustainable approach we have to improve capabilities to a level to support productive projects
  - Secure long term funding by MPW & Foundry Service
  - Achieve industrial/non-public funding

Free MPW Runs - support open source PDK & design

- Table provides schedule of MPW Runs for FMD-QNC project and planed usage of CoreExpert group and open community

	Jun 23	Dez 23	Jun 24	Dez 24	Apr 25	Jun 25	Dez 25
Fläche [mm²]		25	40	50	**280**	60	65
Anteil Design Akademie							
CoreExpert Group		**25**	**30**	**30**	**140**	**30**	**30**
open community		0	10	20	**140**	30	35
ToolBasis							
commerial tools (in %)		**50**	**50**	**50**	**30**	**20**	**20**
open source tools (in %)		**50**	**50**	**50**	**70**	**80**	**80**

- Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others.
- In the project, a continuation for the provision of free area for the open source community is to be worked out.
- Goal is to cooperate with IIS / Europractice

Free MPW Runs - support open source PDK & design

- Flow for designs from open source community

1) Specification / Criteria desired IP

2) Community provides designs open source

3) Production of selected open source designs

4) Characterization and provision of the IP documentation

1) At the beginning specifications an criteria will be defined by PDK status, later specifications from sponsors might be possible
2) The community can provide designs intended for prototyping via a pull request on an IHP GitHup repository
3) Designs will be selected according to the criteria to be developed in 1) and the available space.
4) Depending on the requirements, characterization can be done in scientific collaborations by the open community which may wish to use the designs for development and research projects.

Open Source Roadmap

- Agree on common goals for a design flow – to channel effort
- Synchronize efforts and tasks
- Leveraging community efforts, public funding and corporate contributions.

- Demonstration of successful open source designs
- Demonstration of design training courses in academic institutions
- Example for a commercial successful project

Workshop – Goals (IHP -view)

- This work shop is not really for free – we want to introduce/promote our goals and ask for cooperation
- Develop Open Source Designs - education of a chip design engineers
- Push Open Source Tools - user-friendly with short learning curve, but enough features
- Networking / Panel Discussion / Wrap up: Adapt / fine-tune our open PDK roadmap

Acknowledgment

- Thanks to discussion platform - Open source semiconductors for EU sovereignty - organized by Matthew Venn
- Thanks to different public founded German projects:

  VE-HEP (16KIS1339K) https://elektronikforschung.de/projekte/ve-hep-1

  IHP Open130-G2 (16ME0852) https://www.elektronikforschung.de/projekte/ihp-open130-g2

  FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc

  Workshop funding - FMD-QNC with VDI/VDE (project management agency) approval

SPONSORED BY THE

Federal Ministry of Education and Research

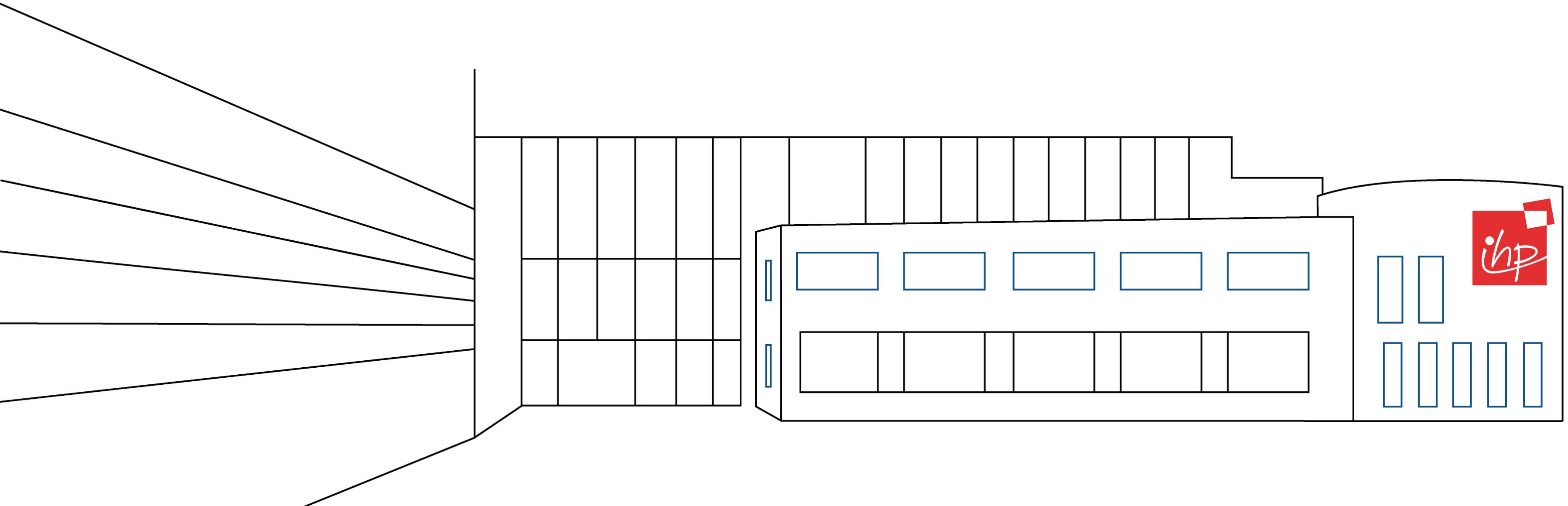
Forschungsfabrik Mikroelektronik Deutschland

Reference list for slide 6:

1) J. Singh et al., Symposium on VLSI Technology, 2017, pp. T140-T14
2) W. Chakraborty et al., Symposium on VLSI Technology, 2021, pp. 1-2.
3) L. Nyssens et al., IEEE Journal of the Electron Devices Society, vol. 8, pp. 646-654, 2020,
4) I. Post et al., IEEE International Electron Devices Meeting, 2006, pp. 1-3
5) H. Li et al., IEEE Symposium on VLSI Technology, 2007, pp. 56-57,
6) B. Heinemann et al, *(2016),* IEEE International Electron Devices Meeting, pp. 3.1.1-3.1.4,
7) H. Rücker et al., 2019, BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)
8) V. Jain et al. 2022, IEEE International Electron Devices Meeting, pp. 11.6
9) P. Chevalier et al., 2014 IEEE International Electron Devices Meeting, 2014, pp. 3.9.1-3.9.3

Thank you for your attention!

IHP – Leibniz-Institut for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Tel.: +49 (0) 335 5625 647
E-Mail: scholz@ihp-microelectronics.com



Forschungsfabrik Mikroelektronik Deutschland

Leibniz Association